

Abstract

An object of the present invention is to provide a technique suitable for achieving low wiring resistance and reducing a variation in the resistance value between semiconductor elements to be multilayered in a method of manufacturing a semiconductor device in which the semiconductor elements are multilayered through laminating semiconductor wafers via an adhesive layer. The method of the present invention includes first to third processes. In the first process, a wafer laminate Y is prepared, the wafer laminate Y having a laminated structure including a wafer 3, wafers 1T with a thickness from 1 to 20 μm , and an adhesive layer 4 with a thickness from 0.5 to 4.5 μm interposed between a main surface 3a of the wafer 3 and a back surface 1b of the wafer 1T. In the second process, holes extending from the main surface 1a of the wafer 1T and reaching a wiring pattern of the wafer 3 are formed by a predetermined etching treatment. In the third process, the holes are filled with a conductive material to form through electrodes. The adhesive layer 4 has an etching rate of 1 to 2 $\mu\text{m}/\text{min}$ in dry etching performed using an etching gas containing CF_4 , O_2 , and Ar at a volume ratio of 100:400:200 under predetermined conditions.