

WHAT IS CLAIMED IS:

1. A method of manufacturing an image sensing apparatus, the method comprising:

forming a first substrate structure including a first region of a pixel region, the first substrate structure having a first surface and a second surface opposite the first surface;

forming a second substrate structure including a circuit region for driving the pixel region, the second substrate structure having a third surface and a fourth surface opposite the third surface;

bonding the first substrate structure to the second substrate structure, such that the first surface of the first substrate structure is connected to the third surface of the second substrate structure;

forming a second region of the pixel region on the second surface of the first substrate structure, subsequent to the bonding of the first substrate structure to the second substrate structure;

forming a first connection via, the first connection via extending from the second surface of the first substrate structure to pass through the first substrate structure;

mounting semiconductor chips including memory chips on the fourth surface of the second substrate structure, using a conductive bump, subsequent to the bonding of the first substrate structure to the second substrate structure;

separating a stack structure of the first substrate structure, the second substrate structure, and the semiconductor chips into unit image sensing apparatuses; and

forming a second connection via passing through a first portion of the second substrate structure,

wherein the forming of the second connection via is performed prior to the bonding of the first substrate structure to the second substrate structure, and further includes exposing the second connection via by removing a second portion of the second substrate structure from the fourth surface, subsequent to the forming of the second region of the pixel region.

2. The method as claimed in claim 1, further comprising:

bonding a carrier substrate to the second surface of the first substrate structure, subsequent to the bonding of the first substrate structure to the second substrate structure; and

removing the carrier substrate from the second surface of the first substrate structure.

3. The method as claimed in claim 1, further comprising: forming a redistribution layer and a conductive connection pad on the fourth surface of the second substrate structure, the conductive connection pad being disposed on the redistribution layer and connected to the conductive bump, prior to the mounting of the semiconductor chips.

4. The method as claimed in claim 1, further comprising: forming an encapsulation portion encapsulating the semiconductor chips.

5. The method as claimed in claim 4, further comprising: removing a portion of the encapsulation portion, such that one surface of the semiconductor chips are exposed.

6. The method as claimed in claim 1, wherein the semiconductor chips include:

a redistribution layer disposed on a surface, connected to the fourth surface of the second substrate structure; and

a connection pad disposed on the redistribution layer and connected to the conductive bump.

7. The method as claimed in claim 1, wherein the mounting of the semiconductor chips includes mounting dummy chips, electrically isolated from the circuit region, together with the semiconductor chips.

8. The method as claimed in claim 1, wherein the mounting of the semiconductor chips includes mounting logic chips, electrically connected to the circuit region, together with the semiconductor chips.

9. The method as claimed in claim 1, wherein the second substrate structure includes:

a second substrate having elements disposed thereon to form the circuit region; and

an interlayer insulating layer disposed on the second substrate and having a wiring structure disposed therein,

wherein the first connection via extends to a portion of the interlayer insulating layer.

10. The method as claimed in claim 9, wherein the second connection via passes through the second substrate, and is connected to the wiring structure disposed in the interlayer insulating layer.

11. The method as claimed in claim 10, wherein the first connection via and the second connection via are disposed in different positions on a plane.

12. The method as claimed in claim 1, wherein:

the first substrate structure includes a first substrate, the first substrate having a photoelectric conversion element, and having a fifth surface and a sixth surface,

the first region of the pixel region includes a region formed from the fifth surface of the first substrate, and

the second region of the pixel region includes a region formed from the sixth surface of the first substrate.

13. A method of manufacturing an image sensing apparatus, the method comprising:

forming a first substrate structure including a photoelectric conversion element in a pixel region, the first substrate structure having a first surface and a second surface opposite the first surface;

forming a second substrate structure including a circuit region for driving the pixel region, the second substrate structure having a third surface and a fourth surface opposite the third surface;

bonding the first substrate structure to the second substrate structure, such that the first surface of the first substrate structure is connected to the third surface of the second substrate structure;

forming a color filter and a microlens of the pixel region on the second surface of the first substrate structure, subsequent to the bonding of the first substrate structure to the second substrate structure;

mounting semiconductor chips including memory chips on the fourth surface of the second substrate structure, using a conductive bump, subsequent to the bonding of the first substrate structure to the second substrate structure; and

forming a connection via passing through a first portion of the second substrate structure,

wherein the forming of the connection via is performed prior to the bonding of the first substrate structure to the second substrate structure, and further includes exposing the connection via by removing a second portion of the second substrate structure from the fourth surface, subsequent to the forming of the color filter and the microlens.

14. The method as claimed in claim 13, wherein the mounting of the semiconductor chips includes:

bonding a carrier substrate to the second surface of the first substrate structure;

forming a redistribution layer and a conductive connection pad on the fourth surface of the second substrate structure, the conductive connection pad being disposed on the redistribution layer and connected to the conductive bump;

connecting the semiconductor chips on the fourth surface of the second substrate structure, using the conductive bump;

forming an encapsulation portion encapsulating the semiconductor chips; and

removing the carrier substrate from the second surface of the first substrate structure.

15. The method as claimed in claim 13, wherein the bonding of the first substrate structure to the second substrate structure includes:

forming a first metal connection portion on the first surface of the first substrate structure;

forming a second metal connection portion on the third surface of the second substrate structure; and

bonding the first metal connection portion to the second metal connection portion.

16. The method as claimed in claim 15, wherein the first metal connection portion and the second metal connection portion each have a columnar shape, and the first substrate structure and the second substrate structure are electrically connected by the first metal connection portion and the second metal connection portion.

17. A method of manufacturing an image sensing apparatus, the method comprising:

forming a stack structure of a first substrate structure and a second substrate structure, by bonding the first substrate structure to the second substrate structure, such that a first surface of the first substrate structure is connected to a third surface of the second substrate structure;

wherein the first substrate structure comprises a second surface opposite the first surface, and wherein the second substrate structure comprises a fourth surface opposite the third surface;

wherein the first substrate structure includes a pixel region, and the second substrate structure includes a circuit region for driving the pixel region;

forming a connection via passing through a first portion of the second substrate structure,

wherein the forming of the connection via is performed prior to the bonding of the first substrate structure to the second substrate structure;

bonding a carrier substrate to the second surface of the first substrate structure;

exposing the connection via by removing a second portion of the second substrate structure from the fourth surface, subsequent to the bonding of the first substrate structure to the second substrate structure;

forming a redistribution layer and a conductive connection pad disposed on the redistribution layer, on the fourth surface of the second substrate structure;

connecting semiconductor chips including memory chips on the fourth surface of the second substrate structure, using a conductive bump, subsequent to the forming of the stack structure of the first substrate structure and the second substrate structure;

forming an encapsulation portion encapsulating the semiconductor chips;

removing the carrier substrate from the second surface of the first substrate structure; and

separating a stack structure of the first substrate structure, the second substrate structure, and the semiconductor chips into unit image sensing apparatuses.