

A PROCESSOR SOFTWARE DEVELOPMENT AND TEST APPARATUS

ABSTRACT

A real-time memory monitoring apparatus 10,80 which accesses memory areas and registers of the embedded processor 34 under test while it is executing its program, in order to observe and modify its operating conditions in real-time. Automated tests involving the verification of events using target specifications 19 dependent upon the real-time claim 36 can be performed before the scheduled event is triggered. A database engine 17 documents test cases and probable causes of errors. The standardisation of naming conventions employed in firmware 35 across different processor's 34 eases the transition in the use of one processor to another within a given application. The apparatus 10,80 is capable of targeting processors 34 from different families, thus eliminating the need to acquire multiple emulators. The apparatus 10,80 allows the internal memory locations of the embedded processor 34 under test to be monitored and changed while the processor 34 is executing.

Fig. 1