DUAL-GATE STRUCTURE AND METHOD OF FABRICATING INTEGRATED CIRCUITS HAVING DUAL-GATE STRUCTURES

162162

ABSTRACT

A method of fabricating a dual-gate on a substrate and an integrated circuit having a dual-gate structure are provided. A first high-K dielectric layer is formed in a first area defined for a first gate structure and in a second area defined for a second gate structure. A second high-K dielectric layer is formed in the first and second areas. The first high-K dielectric layer has a lower etch rate to an etchant relative to the second high-K dielectric layer. The second high-K dielectric layer is etched from the second area to said first high-K dielectric layer with the etchant, and a gate conductive layer is formed in the first and second areas over the second high-K dielectric layer and first high-K dielectric layer, respectively.

FIG. 4B