METHODS FOR FABRICATING A STRESSED MOS DEVICE

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention generally relates methods for fabricating stressed MOS devices, and more particularly relates to methods for fabricating stressed MOS devices and for preserving the stress and the stress induced enhancement in such devices.

BACKGROUND OF THE INVENTION

[0002] The majority of present day integrated circuits (ICs) are implemented by using a plurality of interconnected field effect transistors (FETs), also called metal oxide semiconductor field effect transistors (MOSFETs), or simply MOS transistors. An MOS transistor includes a gate electrode as a control electrode and spaced apart source and drain electrodes between which a current can flow. A control voltage applied to the gate electrode controls the flow of current through a channel between the source and drain electrodes.

[0003] MOS transistors, in contrast to bipolar transistor, are majority carrier devices. The gain of an MOS transistor, usually defined by the transconductance (g_m), is proportional to the mobility of the majority carrier in the transistor channel. The current carrying capability of an MOS transistor is proportional to the mobility of the majority carrier in the channel. The mobility of holes, the majority carrier in a P-channel MOS transistor can be increased by applying a compressive longitudinal stress to the channel. The mobility of electrons, the majority carrier in an N-channel MOS transistor can be increased by applying a tensile transverse stress to the channel. In a silicon MOS transistor such stresses can be applied to the channel of an MOS transistor by appropriately embedding a stress inducing material such as SiGe in the silicon substrate of the transistor. The stresses are caused by lattice mismatches between the SiGe and the host silicon material. The intrinsic stresses in the SiGe redistribute into the adjacent areas of the host substrate, namely into the channel region of the MOS transistor. Unfortunately, one of the problems with embedded SiGe technology is the mechanical stability of the SiGe layers. At elevated temperatures the intrinsic stress in the SiGe layers relaxes due to dislocation generation. The decrease in stress, in turn, causes a reduction in the stress induced mobility increase, and hence a deterioration of device performance.

[0004] Accordingly, it is desirable to provide methods for fabricating stressed MOS devices that prevent stress relaxation. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and the foregoing technical field and background.

BRIEF SUMMARY OF THE INVENTION

[0005] A method for fabricating a stressed MOS device in and on a semiconductor substrate is provided. The method comprises the steps of forming a gate electrode overlying the semiconductor substrate and etching a first trench and a second trench in the semiconductor substrate, the first trench and the second trench formed in alignment with the gate electrode. A stress inducing material is selectively grown in the first trench and in the second trench and conductivity determining impurity ions are implanted into the stress inducing material to form

a source region in the first trench and a drain region in the second trench. To preserve the stress induced in the substrate, a layer of mechanically hard material is deposited overlying the stress inducing material after the step of ion implanting.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and wherein FIGS. 1-6 schematically illustrate, in cross section, a stressed MOS device and methods for its fabrication in accordance with various embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0007] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0008] FIGS. 1-6 illustrate a stressed MOS device 30 and method steps for fabricating such an MOS device in accordance with various embodiments of the invention. In this illustrative embodiment stressed MOS device 30 is illustrated by a single P-channel MOS transistor. An integrated circuit formed from stressed MOS devices such as device 30 can include a large number of such transistors, and may also include unstressed P-channel MOS transistors and stressed and unstressed N-channel transistors as well.

[0009] Various steps in the manufacture of MOS transistors are well known and so, in the interest of brevity, many conventional steps will only be mentioned briefly herein or will be omitted entirely without providing the well known process details. Although the term "MOS device" properly refers to a device having a metal gate electrode and an oxide gate insulator, that term will be used throughout to refer to any semiconductor device that includes a conductive gate electrode (whether metal or other conductive material) that is positioned over a gate insulator (whether oxide or other insulator) which, in turn, is positioned over a semiconductor substrate.

[0010] As illustrated in FIG. 1, the manufacture of a stressed MOS device 30 in accordance with an embodiment of the invention begins with providing a semiconductor substrate 36. The semiconductor substrate is preferably a monocrystalline silicon substrate wherein the term "silicon substrate" is used herein to encompass the relatively pure silicon materials typically used in the semiconductor industry. Semiconductor substrate 36 will herein be referred to, for ease of discussion but without limitation, alternatively as a silicon substrate or as a semiconductor substrate. Silicon substrate 36 may be a bulk silicon wafer or a thin layer of silicon on an insulating layer (commonly know as silicon-on-insulator or SOI) that, in turn, is supported by a silicon carrier wafer, but is here illustrated, without limitation, as a bulk silicon wafer. Preferably the silicon wafer has (100) or (110) orientation and at least the portion of the wafer in which MOS device 30 is to be fabricated is doped with N-type impurity dopants (for example, an N-well). The N-well can be doped to the appropriate conductivity, for example, by ion implantation. Shallow trench isolation (STI) (not illustrated) is formed in the semiconductor substrate to electrically isolate individual devices as required by the circuit function being implemented. As is well known, there are many processes that can be used to form the STI, so the process need not be described here

in detail. In general, STI includes a shallow trench that is etched into the surface of the semiconductor substrate and that is subsequently filled with an insulating material. After the trench is filled with the insulating material, the surface is usually planarized, for example by chemical mechanical planarization (CMP).

[0011] A layer of gate insulator 60 is formed on the surface of silicon substrate 36. The gate insulator may be a thermally grown silicon dioxide formed by heating the silicon substrate in an oxidizing ambient, or may be a deposited insulator such as a silicon oxide, silicon nitride, a high dielectric constant insulator such as HfSiO, or the like. Deposited insulators can be deposited by chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD). The gate insulator material is typically 1-10 nanometers (nm) in thickness. In accordance with one embodiment of the invention a layer of polycrystalline silicon 62 is deposited onto the layer of gate insulator. The layer of polycrystalline silicon is preferably deposited as undoped polycrystalline silicon and is subsequently impurity doped by ion implantation. A layer 64 of hard mask material such as silicon oxide, silicon nitride, or silicon oxynitride can be deposited onto the surface of the polycrystalline silicon. The polycrystalline material can be deposited to a thickness of about 100 nm by LPCVD by the hydrogen reduction of silane. The hard mask material can be deposited to a thickness of about 50 nm, also by LPCVD.

[0012] Hard mask layer 64 and underlying layer of polycrystalline silicon 62 are photolithographically patterned to form a P-channel MOS transistor gate electrode 66 as illustrated in FIG. 2. Gate electrode 66 overlies the portion of semiconductor substrate 36 that will form channel 68 of P-channel MOS transistor 30. The polycrystalline silicon can be etched in the desired pattern by, for example, plasma etching in a Cl or HBr/O_2 chemistry and the hard mask can be etched, for example, by plasma etching in a CHF_3, CF_4, or SF_6 chemistry. Following the patterning of the gate electrode, in accordance with one embodiment of the invention, a thin layer 70 of silicon oxide is thermally grown on the opposing sidewalls 72 of gate electrode 66 by heating the polycrystalline silicon in an oxidizing ambient. Layer 70 can be grown to a thickness of about 2-5 nm. Gate electrode 66 and layer 70 can be used as an ion implant mask to form source and drain extensions (not illustrated) of the MOS transistor. The possible need for and method of forming multiple source and drain regions are well known, but are not germane to this invention and hence need not be explained herein.

[0013] In accordance with one embodiment of the invention, as illustrated in FIG. 3, sidewall spacers 80 are formed on the opposing sidewalls 72 of gate electrode 66. The sidewall spacers can be formed of silicon nitride, silicon oxide, or the like by depositing a layer of the spacer material over the gate electrodes and subsequently anisotropically etching the layer, for example by reactive ion etching. Sidewall spacers 80, gate electrode 66, and the hard mask on the top of the gate electrode are used as an etch mask to etch trenches 82 and 84 in the silicon substrate in spaced apart self alignment with P-channel gate electrode 66. The trenches intersect the ends of channel 68. The trenches can be etched, for example, by plasma etching using a Cl or HBr/O_2 chemistry. Preferably each of the trenches has a depth or about 0.04-0.2 μm.

[0014] As illustrated in FIG. 4, the trenches are filled with a layer of stress inducing material 90. The stress inducing material can be any monocrystalline material that can be grown on the silicon substrate with a different lattice constant than the lattice constant of silicon. The difference in lattice constant of the two juxtaposed materials generates a stress at the interface between the two materials that is redistributed in the host material.

Preferably the stress inducing material causes the silicon host to deform elastically so that the silicon is stressed, but remains a substantially defect free perfect crystal. Defects can cause a decrease or relief of the stress. The stress inducing material can be, for example, monocrystalline silicon germanium (SiGe) having about 10-25 atomic percent germanium or monocrystalline silicon containing about 1-4 atomic percent of substitutional carbon and preferably less than about 2 atomic percent substutional carbon. Preferably the stress inducing material is epitaxially grown by a selective growth process. Methods for epitaxial growth of these materials on a silicon host in a selective manner are will known and need not be described herein. In the case of SiGe, for example, the SiGe has a lattice constant greater than the lattice constant of silicon, and this creates a compressive longitudinal stress in transistor channel 68. The compressive longitudinal stress increases the mobility of holes in channel 68 and hence improves the performance of a P-channel MOS transistor.

[0015] Following the growth of the stress inducing material in trenches 82 and 84, P-type conductivity determining ions are implanted into the stress inducing material as indicated by arrows 86 to form a source region 92 and a drain region 94 of P-channel MOS transistor 30 as illustrated in FIG. 5. To become electrically active, the implanted ions must be annealed, and such anneal is usually carried out soon after the implantation is completed. Elevated temperatures, however, cause intrinsic stresses in the SiGe or other stress inducing material to relax due to the generation of dislocations that are nucleated on the surface and the creation of steps at the surface of the SiGe.

[0016] In accordance with an embodiment of the invention, as illustrated in FIG. 6, the relaxation of stress in channel 68 is prevented by depositing a layer 96 with high mechanical strength onto the surface of the stress inducing material. The layer of high mechanical strength retards step formation and prevents dislocation nucleation and propogation at the surface of the stress inducing material. The layer of high mechanical strength is applied before the annealing of the ion implantation or any other high temperature steps. After application of layer 96 the device can be subjected to high temperatures and the stress will be preserved. Layer 96 can be any material that can be deposited at a relatively low temperature and that has a Young's modulus greater than and preferably much greater than the Young's modulus of the stress inducing material. For example, for use with SiGe which has a Young's modulus of about 150 GPa, silicon nitride (Young's modulus about 350 GPa), silicon carbide (Young's modulus between about 400 and 750 GPa) and diamond-like carbon (Young's modulus up to 800 GPa) are suitable materials for layer 96. As used herein, low temperature means any temperature less than about 600°C, and high temperature means any temperature greater than about 900°C. Layer 96 can be deposited by CVD, LPCVD, or PECVD. A layer of silicon nitride can be deposited, for example by PECVD at a temperature of about 450°C by the plasma enhanced reaction of dichlorosilane and ammonia. Similarly, silicon carbide can be deposited by using the vapor phase $SiCl_4$ and methane at 550°C and PECVD diamond-like carbon can be deposited using a gas mixture of Ar, H_2, SiH_4 and C_2H_2 at 200°C. It may be advantageous, in accordance with an alternate embodiment of the invention (not illustrated), to first provide a layer of pad oxide having a thickness of, for example, 2-5nm beneath layer 96 of high mechanical strength. The layer of pad oxide serves to prevent any reaction between, for example, the silicon nitride and the underlying semiconductor material.

[0017] Stressed MOS device 30 can be completed by well known steps (not illustrated) such as depositing a layer of dielectric material over layer 96, etching opening through the dielectric material and layer 96 to expose portions of the source and drain regions, and forming metallization that extends through the openings to

electrically contact the source and drain regions. Further layers of interlayer dielectric material, additional layers of interconnect metallization, and the like may also be applied and patterned to achiever the proper circuit function of the integrated circuit being implemented.

[0018] While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the exemplary embodiment or exemplary embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope of the invention as set forth in the appended claims and the legal equivalents thereof.

CLAIMS

1. A method for fabricating a stressed MOS device [30] comprising the steps of:

providing a monocrystalline semiconductor substrate [36];

etching a trench [82] into the monocrystalline semiconductor substrate [36];

selectively filling the trench [82] with a monocrystalline semiconductor material [90] that is lattice mismatched with the monocrystalline semiconductor substrate [36], the monocrystalline semiconductor material [90] having a first Young's modulus; and

depositing a film of material [96] having a second Young's modulus greater than the first Young's modulus in contact with the monocrystalline semiconductor material [90], wherein the film of material [96] is designed to preserve a stress condition caused by the monocrystalline semiconductor material [90] in the monocrystalline semiconductor substrate [36] during subsequent processing, the step of depositing a film of material [96] occurring before the monocrystalline semiconductor material is heated to a temperature greater than about 600°C.

2. The method of claim 1 wherein the step of providing a monocrystalline substrate [36] comprises the step of providing a monocrystalline silicon substrate and the step of selectively filling the trench comprises the step of selectively filling the trench with a monocrystalline material [90] selected from the group consisting of monocrystalline SiGe and monocrystalline silicon containing at least 2% carbon.