

DESCRIPTION**MEMORY ARRAYS AND METHODS USED IN FORMING A MEMORY
ARRAY COMPRISING STRINGS OF MEMORY CELLS AND
OPERATIVE THROUGH-ARRAY-VIAS**

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TECHNICAL FIELD

Embodiments disclosed herein pertain to memory arrays and to methods used in forming a memory array comprising strings of memory cells and operative through-array-vias.

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BACKGROUND

Memory is one type of integrated circuitry and is used in computer systems for storing data. Memory may be fabricated in one or more arrays of individual memory cells. Memory cells may be written to, or read from, using digitlines (which may also be referred to as bitlines, data lines, or sense lines) and access lines (which may also be referred to as wordlines). The sense lines may conductively interconnect memory cells along columns of the array, and the access lines may conductively interconnect memory cells along rows of the array. Each memory cell may be uniquely addressed through the combination of a sense line and an access line.

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Memory cells may be volatile, semi-volatile, or non-volatile. Non-volatile memory cells can store data for extended periods of time in the absence of power. Non-volatile memory is conventionally specified to be memory having a retention time of at least about 10 years. Volatile memory dissipates and is therefore refreshed/rewritten to maintain data storage. Volatile memory may have a retention time of milliseconds or less. Regardless, memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store more than two levels or states of information.

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A field effect transistor is one type of electronic component that may be used in a memory cell. These transistors comprise a pair of conductive source/drain regions having a semiconductive channel region there-between. A conductive gate is adjacent the channel region and separated there-from by a thin gate insulator. Application of a suitable voltage to the gate allows

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current to flow from one of the source/drain regions to the other through the channel region. When the voltage is removed from the gate, current is largely prevented from flowing through the channel region. Field effect transistors may also include additional structure, for example a reversibly programmable charge-storage region as part of the gate construction
5 between the gate insulator and the conductive gate.

Flash memory is one type of memory and has numerous uses in modern computers and devices. For instance, modern personal computers may have BIOS stored on a flash memory chip. As another example, it is
10 becoming increasingly common for computers and other devices to utilize flash memory in solid state drives to replace conventional hard drives. As yet another example, flash memory is popular in wireless electronic devices because it enables manufacturers to support new communication protocols as they become standardized, and to provide the ability to remotely upgrade
15 the devices for enhanced features.

NAND may be a basic architecture of integrated flash memory. A NAND cell unit comprises at least one selecting device coupled in series to a serial combination of memory cells (with the serial combination commonly being referred to as a NAND string). NAND architecture may be configured
20 in a three-dimensional arrangement comprising vertically-stacked memory cells individually comprising a reversibly programmable vertical transistor. Control or other circuitry may be formed below the vertically-stacked memory cells. Other volatile or non-volatile memory array architectures may also comprise vertically-stacked memory cells that individually
25 comprise a transistor.

Memory arrays may be arranged in memory pages, memory blocks and partial blocks (e.g., sub-blocks), and memory planes, for example as shown and described in any of U.S. Patent Application Publication Nos. 2015/0228659, 2016/0267984, and 2017/0140833, and which are hereby and
30 herein fully incorporated by reference and aspects of which may be used in some embodiments of the inventions disclosed herein.

One proposed way of increasing integrated circuitry density is to form a three-dimensional (3D) array comprising tiers of electronic components, for example tiers of non-programmable transistors and/or programmable
35 transistors that may be part of memory circuitry. The gates of such

transistors may be patterned into gate lines (and which may be plate-like) in the individual tiers. Connections to these gate lines may occur in a so-called “stair-step structure” at an end or edge of the tiers of transistors or other electronic components. The stair-step structure includes individual “stairs”
5 (alternately termed “steps” or “stair-steps”) that define contact regions of the individual gate lines upon which elevationally-extending conductive vias contact to provide electrical access to the gate lines or other conductive structures.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1 is a diagrammatic top plan view of a die or die area that may be part of a larger substrate (not shown; e.g., a semiconductor wafer).

Fig. 2 is an enlarged diagrammatic top view of a portion of Fig. 1 of a portion of a substrate in process in accordance with an embodiment of the
15 invention and is taken through line 2-2 in Fig. 1.

Figs. 3-121 are diagrammatic sequential sectional and/or enlarged views of the construction of Fig. 1 in process in accordance with some embodiments of the invention.

20 **DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS**

Embodiments of the invention encompass methods used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs; i.e., that contain conductive material and that are circuit-operative in a finished-circuitry construction). An example memory
25 array is an array of NAND or other memory cells having peripheral control circuitry under the array (e.g., CMOS-under-array). Embodiments of the invention encompass so-called “gate-last” or “replacement-gate” processing, so-called “gate-first” processing, and other processing whether existing or future-developed independent of when transistor gates are formed.

Embodiments of the invention also encompass a memory array (e.g., NAND architecture) independent of method of manufacture. First example method embodiments are described with reference to Figs. 1-121 which may be considered as a “gate-last” or “replacement-gate” process. Further, and
30 regardless, the following sequence of processing steps is but one example and other sequences of the example processing steps (with or without other
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processing steps) may be used regardless of whether using “gate-last/replacement-gate” processing.

Fig. 1 shows an example diagrammatic embodiment comprising a die or die area 100 that may be part of a larger substrate (e.g., a semiconductor wafer, and not shown) and within which a memory array will be fabricated. Example die area 100 comprises at least one memory plane 105 (four being shown), a stair-step region 60 (two being shown), and a peripheral circuitry region PC (two being shown). Regions 105, 60, and/or PC may not be discernable at this point of processing. Figs. 2-15 are diagrammatic larger and varied scale views of portions of die area 100.

Figs. 2-15 show a construction 10 in a method of forming an array 12 of elevationally-extending strings of transistors and/or memory cells (not yet shown). Construction 10 comprises a base substrate 11 having any one or more of conductive/conductor/conducting, semiconductive/semiconductor/semiconducting, or insulative/insulator/insulating (i.e., electrically herein) materials. Various materials have been formed elevationally over base substrate 11. Materials may be aside, elevationally inward, or elevationally outward of the Figs. 2-15-depicted materials. For example, other partially or wholly fabricated components of integrated circuitry may be provided somewhere above, about, or within base substrate 11. Control and/or other peripheral circuitry for operating components within an array (e.g., array 12) of elevationally-extending strings of memory cells may also be fabricated and may or may not be wholly or partially within an array or sub-array. Further, multiple sub-arrays may also be fabricated and operated independently, in tandem, or otherwise relative one another. In this document, a “sub-array” may also be considered as an array.

Example construction 10 comprises a conductor tier 16 that has been formed above substrate 11. Example conductor tier 16 is shown as comprising conductive material 17 (e.g., conductively-doped semiconductive material such as conductively-doped polysilicon) above metal material 19 (e.g., WSi_x). Conductor tier 16 may comprise part of control circuitry (e.g., peripheral-under-array/CMOS-under-array circuitry) used to control read and write access to the transistors and/or memory cells that will be formed within array 12.

Construction 10 comprises a stack 18 above conductor tier 16. Stack 18 comprises vertically-alternating insulative tiers 20 and conductive tiers 22. Example thickness for each of tiers 20 and 22 is 22 to 60 nanometers. Only a small number of tiers 20 and 22 is shown, with more likely stack 18 comprising dozens, a hundred or more, etc. of tiers 20 and 22. Other circuitry that may or may not be part of peripheral and/or control circuitry may be between conductor tier 16 and stack 18. For example, multiple vertically-alternating tiers of conductive material and insulative material of such circuitry may be below a lowest of the conductive tiers 22 and/or above an uppermost of the conductive tiers 22. For example, one or more select gate tiers (not shown) may be between conductor tier 16 and the lowest conductive tier 22 and one or more select gate tiers may be above an uppermost of conductive tiers 22. Regardless, conductive tiers 22 may not comprise conductive material and insulative tiers 20 may not comprise insulative material or be insulative at this point in processing. Example conductive tiers 22 comprise first material 26 (e.g., silicon nitride) which may be wholly or partially sacrificial. Example insulative tiers 20 comprise second material 24 (e.g., silicon dioxide) that is of different composition from that of first material 26 and which may be wholly or partially sacrificial.

Stack 18 comprises a through-array-via (TAV) region (e.g., any one of TAV regions 21, 21A, 21B) and an operative memory-cell-string region 23. An “operative memory-cell string region” contains circuit-operative memory-cell strings in the finished construction of integrated circuitry that has been or is being fabricated. Dummy memory-cell strings (i.e., circuit-inoperative memory-cell strings, and not shown) may be between the TAV region and operative memory-cell-string region 23. TAV regions 21, 21A, 21B comprise spaced operative TAV areas 27. A “TAV region” is a region containing multiple operative TAV areas. An “operative TAV area” is an area in which an operative TAV is present or will be formed. An “operative TAV” is a circuit-operative conductive interconnect extending through stack 18 and between electronic components at different elevations in a finished construction of integrated circuitry that has been or is being fabricated. Regions 23 and 21/21A/21B and areas 27 may essentially be undefined or indistinguishable relative one another in construction 10 at this

point in processing. Example TAV regions 21 are shown as being within individual memory planes 105 (Fig. 1). TAV region 21A is shown as being outside of individual memory planes 105 with, in one example, shown as being edge-of-plane (i.e., outside of a memory plane and adjacent a lateral edge of the subject memory plane).

In one example and for ease of depiction in the drawings, TAV region 21B is shown as being within a landing region 62 of an individual stair-step region 60. One landing region 62 is shown as being immediately-adjacent operative memory-cell-string region 23 and having operative TAV areas 27 therein. Alternately, a landing region 62 that is immediately adjacent or part of operative memory-cell-string region 23 may have no operative TAV areas 27 therein (not shown), and/or have operative TAV areas 27 that are in part of another landing region 62 that is spaced from operative memory-cell-string region 23 (not shown, and further described below).

Referring to Figs. 16-27, and in one embodiment, operative channel openings 25 and dummy channel openings 67 have been etched through insulative tiers 20 and conductive tiers 22 to material 17 of conductor tier 16, with in one example dummy channel openings being in each of TAV regions 21, 21A, and 21B. An “operative channel opening” is an opening in which circuit-operative channel material of a transistor and/or memory cell is or will be received. A “dummy channel opening” is an opening in which circuit-inoperative channel material is or will be received, with such circuit-inoperative channel material if in a finished-circuitry construction being circuit-inoperative, meaning no current flow there-through and which may be a circuit-inoperable dead-end that is not part of a current flow path of a circuit even if extending to or from an electronic component. In one embodiment, dummy channel openings 67 may be formed within operative TAV areas 27 (not shown) and in another embodiment no dummy channel openings 67 are formed within operative TAV areas 27 (as shown). In embodiments where dummy channel openings are formed in TAV region 21B having a stair-step region 60, such may not necessarily be formed in the one landing region 62 that is immediately-adjacent operative memory-cell-string region 23. For example, a landing region 62 that is immediately adjacent or part of operative memory-cell-string region 23 may

have no dummy channel openings therein (not shown), and/or have dummy channel openings that are in part of another landing region 62 that is spaced from operative memory-cell-string region 23 (not shown, and further described below).

5 Operative channel openings 25 and/or dummy channel openings 67 may go partially into material 17 (not shown), may stop there-atop as shown, or go completely there-through (not shown) either stopping on material 19 or going at least partially there-into. Alternately, as an example, operative channel openings 25 and/or dummy channel openings 67 may stop
10 atop or within lowest insulative tier 20. A reason for extending operative channel openings 25 at least to material 17 is to assure direct electrical coupling of subsequently-formed channel material (not yet shown) to conductor tier 16 without using alternate processing and structure to do so when such a connection is desired. Etch-stop material (not shown) may be
15 within conductive material 17 to facilitate stopping of the etching of openings 25 and 67 to be atop conductor tier 16 when such is desired. Such etch-stop material may be sacrificial or non-sacrificial. By way of example only, operative channel openings 25 and dummy channel openings 67 are arranged in groups or columns of staggered horizontal rows or diagonal rows
20 (e.g., in a hexagonal close-pack unit cell of a 2D lattice as shown). Any alternate existing or future-developed arrangement and construction may be used. In one embodiment and as shown, operative channel openings 25 and dummy channel openings 67 are formed to collectively have a common horizontal pitch (e.g., P in Figs. 16, 18, 20, 21, and 25) along parallel
25 horizontally-straight lines. Formation of dummy channel openings 67 “on-pitch” P with operative channel openings 25 may facilitate more uniform patterning of all channel openings 25 and 67 than would otherwise occur if dummy channel openings 67 collectively had a pitch different than P.

30 Transistor channel material may be formed in the individual operative channel openings elevationally along the insulative tiers and the conductive tiers, thus comprising individual operative channel-material strings, which is directly electrically coupled with conductive material in the conductor tier. Transistor channel material may also be formed in the individual dummy
35 channel openings elevationally along the insulative tiers and the conductive

tiers, thus comprising individual dummy channel-material strings (i.e., which if in a finished-circuitry construction being circuit-inoperative, meaning no current flow there-through and which may be a circuit-inoperable dead-end that is not part of a current flow path of a circuit even
5 if extending to or from an electronic component). Individual memory cells (i.e., circuit-operative memory cells) of the example memory array being formed may comprise a gate region (e.g., a control-gate region) and a memory structure laterally between the gate region and the channel material. In one such embodiment, the memory structure is formed to comprise a
10 charge-blocking region, storage material (e.g., charge-storage material), and an insulative charge-passage material. The storage material (e.g., floating gate material such as doped or undoped silicon or charge-trapping material such as silicon nitride, metal dots, etc.) of the individual memory cells is elevationally along individual of the charge-blocking regions. The
15 insulative charge-passage material (e.g., a band gap-engineered structure having nitrogen-containing material [e.g., silicon nitride] sandwiched between two insulator oxides [e.g., silicon dioxide]) is laterally between the channel material and the storage material.

Figs. 28-41 show one embodiment wherein charge-blocking
20 material 30, storage material 32, and charge-passage material 34 have been formed in individual operative channel openings 25 and in individual dummy channel openings 67 elevationally along insulative tiers 20 and conductive tiers 22. Transistor materials 30, 32, and 34 (e.g., memory cell materials) may be formed by, for example, deposition of respective thin
25 layers thereof over stack 18 and within individual operative channel openings 25 followed by planarizing such back at least to an uppermost surface of stack 18. Channel material 36 has been formed in operative channel openings 25 and in dummy channel openings 67 elevationally along insulative tiers 20 and conductive tiers 22, thus comprising individual
30 operative channel-material strings 53 in operative memory-cell-string region 23 and dummy channel-material strings 35 in the TAV region (e.g., in any one or more of regions 21, 21A, 21B, and laterally outside of and not within operative TAV areas 27). Example channel materials 36 include appropriately-doped crystalline semiconductor material, such as one or more
35 silicon, germanium, and so-called III/V semiconductor materials (e.g.,

GaAs, InP, GaP, and GaN). Example thickness for each of materials 30, 32, 34, and 36 is 25 to 100 Angstroms. Punch etching may be conducted as shown to remove materials 30, 32, and 34 from the bases of operative channel openings 25 to expose conductor tier 16 such that channel material 36 is directly against conductive material 17 of conductor tier 16. Alternately, and by way of example only, no punch etching may be conducted and channel material 36 in operative channel openings 25 may be directly electrically coupled to material 17/19 by a separate conductive interconnect (not shown). Operative channel openings 25 and dummy channel openings 67 are shown as comprising a radially-central solid dielectric material 38 (e.g., spin-on-dielectric, silicon dioxide, and/or silicon nitride). Alternately, and by way of example only, the radially-central portion within operative channel openings 25 and dummy channel openings 67 may include void space(s) (not shown) and/or be devoid of solid material (not shown).

Referring to Figs. 42 and 43, and in one embodiment, a stair-step structure 64 (e.g., having steps 63) has been formed into stack 18 in stair-step region 60 and a landing (e.g., 66X and/or 66Z, with 66X being a landing crest and 66Z being a landing foot) has been formed in landing region 62 of stair-step region 60. Alternately, no landing 66X may be immediately-adjacent memory-cell-string region 23 (not shown), with for example an uppermost step 63 (not shown) being immediately there-adjacent. Stair-step structure 64 in the example “gate-last” method is circuit-inoperative but will comprise an operative stair-step structure in a finished-circuitry construction. An “operative stair-step structure” is circuit-operative having at least some conductive step thereof that electrically couples with and between a) an electronic component in operative memory-cell-string region 23, such as a transistor and/or memory cell, and b) an electronic component outside of operative memory-cell-string region 23. Such an operative stair-step structure may be formed by any existing or later-developed method(s). As one such example, a masking material (e.g., a photo-imageable material such as photoresist) may be formed atop stack 18 and an opening formed there-through. Then, the masking material may be used as a mask while etching (e.g., anisotropically) through the opening to extend such opening into the outermost two tiers 20,

22. The resultant construction may then be subjected to a successive alternating series of lateral-trimming etches of the masking material followed by etching deeper into stack 18 two-tiers 20, 22 at a time using the trimmed masking material having a successively widened opening as a mask. Such an example may result in the forming of stair-step structure 64 into stack 18 that comprises vertically alternating tiers 20, 22 of different composition materials 24, 26, and in the forming of another stair-step structure (not shown) opposite and facing stair-step structure 64 (e.g., in mirror image). Such opposite stair-step structure (not shown) may be a dummy stair-step structure. A “dummy stair-step structure” is circuit-inoperative having steps thereof in which no current flows in conductive material of the steps and which may be a circuit-inoperable dead end that is not part of a current flow path of a circuit even if extending to or from an electronic component. Multiple operative stair-step structures (not shown) and multiple dummy stair-step structures (not shown) may be formed, for example longitudinally end-to-end in different portions of stair-step region 60 and to different depths within stack 18 (not shown). Pairs of opposing mirror-image operative and dummy stair-step structures may be considered as defining a stadium (e.g., a vertically recessed portion having opposing flights of stairs, and not shown).

Referring to Figs. 44-53, operative TAVs 45 have been formed in individual spaced operative TAV areas 27 in one or more of TAV regions 21, 21A, and 21B. If any dummy channel-material strings 35 were formed in operative TAV areas 27 (not shown), such may inherently be replaced by operative TAVs 45. One or more circuit-operative conductive vias 39 have been formed to each step 63. Insulative material 37 (e.g., silicon dioxide) may be formed atop stair-step structure 64 prior to forming operative TAVs 45 and vias 39. Example operative TAVs 45 and vias 39 are shown as comprising a conductive material core 59 surrounded by dielectric material 61 (e.g., silicon dioxide and/or silicon nitride). Regardless, in one embodiment and as shown, the landing below and/or through which dummy channel-material strings 35 and operative TAVs 45 are received is a crest of what-will-be operative stair-step structure 64 (e.g., landing crest 66X). Additionally, or alternately, the landing below and/or through which the dummy channel-material strings and the operative TAVs may be received is

a landing foot of what-will-be operative stair-step structure 64 (e.g., landing foot 66Z and not shown).

Dummy channel-material strings and operative TAVs may additionally or alternately be in other landing crests and/or in other landing foots and, if
5 so, not necessarily be in all landing crests or in all landing foots. Also as referred to above, the dummy channel material openings (now having dummy channel-material strings 35 therein) need not and may not be in the one landing region 62 that is immediately-adjacent operative memory-cell-string region 23. For example, a landing region 62 that is immediately
10 adjacent or part of operative memory-cell-string region 23 may have no dummy channel-material strings therein (not shown), and/or have dummy channel-material strings that are in part of another landing region 62 (a crest and/or a foot) that is spaced from operative memory-cell-string region 23 (not shown). Thereby, operative channel-material strings 53 may be in crest
15 66X in the absence of any operative TAVs and/or dummy channel material strings therein (not shown).

The above example processing shows forming the operative and dummy channel-material strings at the same time and forming the operative TAVs after forming the operative and dummy channel-material strings. In
20 one embodiment, the operative and dummy channel-material strings are formed to individually have the same horizontal shape relative one another and in one embodiment to have the same size and shape relative one another. In one embodiment and as shown, operative channel-material strings 53 and dummy channel-material strings 35 are formed to have the same pitch P
25 relative one another (Fig. 44). In one embodiment and as shown, the operative and dummy channel-material strings are formed to individually be horizontally smaller than the operative TAVs. In one embodiment, operative channel-material strings 53 are within laterally-spaced memory blocks (e.g. memory blocks 115 in Fig. 107) that comprise part of an individual memory
30 plane 105. In one such embodiment, dummy channel-material strings 35, TAV region 21, and operative TAVs 45 are within a memory plane 105. In another embodiment, dummy channel-material strings 35, TAV region 21A and/or 21B, and operative TAVs 45 are outside of a memory plane 105, with in one such embodiment being edge-of-plane (Figs. 107, 115) and in another

such embodiment being in a landing region 62 of a stair-step region 60 (Fig. 118).

Referring to Figs. 54-64, horizontally-elongated trenches 40 have been formed (e.g., by anisotropic etching) through stack 18 to conductor tier
5 16.

Referring to Figs. 65-78, material 26 (not shown) of conductive tiers 22 has been etched selectively relative to materials 24, 30, 32, 34, 36, and 38 (e.g., using liquid or vapor H_3PO_4 as a primary etchant where material 26 is silicon nitride and materials 24, 30, 32, 34, 36, and 38 are polysilicon or other oxides).
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Conducting material is ultimately formed into conductive tiers 22 to comprise conducting material of the individual conductive lines being formed. Referring to Figs. 79-92, such show an example embodiment wherein conducting material 48 has been formed into conductive tiers 22
15 through trenches 40. Any suitable conducting material 48 may be used, for example one or both of metal material and/or conductively-doped semiconductor material. In but one example embodiment, conducting material 48 comprises a first-deposited conformal titanium nitride liner (not shown) followed by deposition of another composition metal material (e.g.,
20 elemental tungsten). A thin insulating material lining (e.g., at least one of Al_2O_3 and HfO_x and not shown) may be formed into conductive tiers 22 through trenches 40 prior to forming conducting material 48.

Referring to Figs. 93-106, conducting material 48 has been removed from individual trenches 40. Such has resulted in formation of conductive
25 lines 29 (e.g., wordlines) and elevationally-extending strings 49 of individual transistors and/or memory cells 56. Such removing may be conducted by etching, for example by one or both of anisotropic etching or isotropic etching. In one isotropic etching example, trenches 40 can be formed to be wider than the vertical depth of individual conductive tiers 22.
30 Conducting material 48 can then be deposited to a thickness that less-than-fills trenches 40 (not shown), for example to leave a laterally-centered void space within trenches 40 (not shown). Thereafter, such conducting material can be isotropically etched within the void space to form conductive lines 29 that are separated as is shown by the Figs. 94
35 and 95 cross-sections. Approximate locations of transistors and/or memory

cells 56 are indicated with a bracket in Fig. 95A and some with dashed outlines in Figs. 94 and 95, with transistors and/or memory cells 56 being essentially ring-like or annular in the depicted example. Conducting material 48 may be considered as having terminal ends 50 (Fig. 95A) corresponding to control-gate regions 52 of individual transistors and/or memory cells 56. Control-gate regions 52 in the depicted embodiment comprise individual portions of individual conductive lines 29. Materials 30, 32, and 34 may be considered as a memory structure 65 that is laterally between control-gate region 52 and channel material 36. A same structure can result with respect to dummy channel-material strings 35 and be dummy (meaning circuit inoperative).

A charge-blocking region (e.g., charge-blocking material 30) is between storage material 32 and individual control-gate regions 52. A charge block may have the following functions in a memory cell: In a program mode, the charge block may prevent charge carriers from passing out of the storage material (e.g., floating-gate material, charge-trapping material, etc.) toward the control gate, and in an erase mode the charge block may prevent charge carriers from flowing into the storage material from the control gate. Accordingly, a charge block may function to block charge migration between the control-gate region and the storage material of individual memory cells. An example charge-blocking region as shown comprises insulator material 30. By way of further examples, a charge-blocking region may comprise a laterally (e.g., radially) outer portion of the storage material (e.g., material 32) where such storage material is insulative (e.g., in the absence of any different-composition material between an insulative storage material 32 and conducting material 48). Regardless, as an additional example, an interface of a storage material and conductive material of a control gate may be sufficient to function as a charge-blocking region in the absence of any separate-composition-insulator material 30. Further, an interface of conducting material 48 with material 30 (when present) in combination with insulator material 30 may together function as a charge-blocking region, and as alternately or additionally may a laterally-outer region of an insulative storage material (e.g., a silicon nitride material 32). An example material 30 is one or more of silicon hafnium oxide and silicon dioxide.

Referring to Figs. 107-121, a material 57 (dielectric and/or silicon-containing such as undoped polysilicon) has been formed in individual trenches 40. A conductive interconnect line (not shown) would operatively electrically couple individual operative TAVs 45, individual vias 5 39, and individual operative channel-material strings 53 to other circuitry (not shown) not particularly material to the inventions disclosed herein.

Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used with respect to the above-described embodiments.

10 In one embodiment and as shown in the drawings referred to above, conducting material of the conductive lines is formed after forming the operative and dummy channel-material strings (e.g., gate-last or replacement-gate processing). Alternately, conducting material of the conductive lines may be formed before forming the operative and dummy 15 channel-material strings (e.g., gate-first processing).

In one embodiment, a method used in forming a memory array (e.g., 12) comprising strings (e.g., 49) of memory cells (e.g., 56) and operative TAVs (e.g., 45) comprises forming a stack (e.g., 18) comprising vertically-alternating insulative tiers (e.g., 20) and conductive tiers (e.g., 20 22). The stack comprises an operative memory-cell-string region (e.g., 23) and a stair-step region (e.g., 60) comprising a landing region (e.g., 62) comprising a TAV region (e.g., 21B). Operative channel-material strings (e.g., 53) are formed in the stack in the operative memory-cell-string region and dummy channel-material strings (e.g., 35) are formed in the stack in the 25 TAV region of the landing region. Operative TAVs (e.g., 45) are formed in the TAV region of the landing region. An operative stair-step structure (e.g., 64) is formed into the stack in the stair-step region and a landing (e.g., 66X and/or 66Z) is formed in the landing region of the stair-step region. In one embodiment, the operative stair-step structure and the landing are formed 30 before forming the operative TAVs. In one embodiment, the operative and dummy channel-material strings are formed before forming the operative stair-step structure and the landing. Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used.

Embodiments of the invention encompass memory arrays independent of method of manufacture. Nevertheless, such memory arrays may have any of the attributes as described herein in method embodiments. Likewise, the above-described method embodiments may incorporate and form any of the attributes described with respect to device embodiments.

In one embodiment, a memory array comprises a vertical stack (e.g., 18) comprising alternating insulative tiers (e.g., 20) and conductive tiers (e.g., 22). The conductive tiers comprise gate regions (e.g., 52) of individual memory cells (e.g., 56) the gate regions individually comprise part of a conductive line (e.g., 29) in individual of the conductive tiers. Operative channel-material strings (e.g., 53) extend through the insulative tiers and the conductive tiers. The individual memory cells comprise a memory structure (e.g., 65) laterally between individual of the gate regions and channel material (e.g., 36) of the operative channel-material strings. An operative stair-step structure (e.g., 64) comprises the insulative tiers and the conductive tiers. A landing region (e.g., 62) is adjacent steps (e.g., 63) of the operative stair-step structure. The landing region comprises a landing (e.g., 66X and/or 66Z) and operative TAVs (e.g., 45) extending through the insulative tier and the conductive tiers. The landing region comprises dummy channel-material strings (e.g., 35) in the insulative tiers and the conductive tiers. Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used.

In one embodiment, CMOS-under-array circuitry is formed. In one such embodiment, the operative TAVs directly electrically couple digitlines of the memory array with CMOS-under-array circuitry, for example as may occur in TAV region 21 where individual operative channel-material strings 53 may inherently comprise a digitline and a conductive interconnect (not shown) directly electrically couples an operative TAV to channel material of a channel-material string. In one embodiment, the memory array comprises NAND.

Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used.

In the inventions disclosed above, other processing, and/or structure may be used as is disclosed in any of U.S. Patent Application Publication No. 2015/0001613; U.S. Patent No. 9,589,978; U.S. Patent Application

Publication No. 2017/0263556; U.S. Patent Application Publication No. 2017/0287833, and U.S. Patent Application Publication No. 2018/0082940. U.S. Patent Application Publication No. 2015/0001613; U.S. Patent No. 9,589,978; U.S. Patent Application Publication No. 5 2017/0287833, and U.S. Patent Application Publication No. 2018/0082940 are herein and hereby incorporated by reference.

The above processing(s) or construction(s) may be considered as being relative to an array of components formed as or within a single stack or single deck of such components above or as part of an underlying base
10 substrate (*albeit*, the single stack/deck may have multiple tiers). Control and/or other peripheral circuitry for operating or accessing such components within an array may also be formed anywhere as part of the finished construction, and in some embodiments may be under the array (e.g., CMOS under-array). Regardless, one or more additional such stack(s)/deck(s) may
15 be provided or fabricated above and/or below that shown in the figures or described above. Further, the array(s) of components may be the same or different relative one another in different stacks/decks. Intervening structure may be provided between immediately-vertically-adjacent stacks/decks (e.g., additional circuitry and/or dielectric layers). Also,
20 different stacks/decks may be electrically coupled relative one another. The multiple stacks/decks may be fabricated separately and sequentially (e.g., one atop another), or two or more stacks/decks may be fabricated at essentially the same time.

The assemblies and structures discussed above may be used in
25 integrated circuits/circuitry and may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems,
30 such as, for example, cameras, wireless devices, displays, chip sets, set top boxes, games, lighting, vehicles, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

In this document unless otherwise indicated, “elevational”, “higher”, “upper”, “lower”, “top”, “atop”, “bottom”, “above”, “below”, “under”,
35 “beneath”, “up”, and “down” are generally with reference to the vertical

direction. “Horizontal” refers to a general direction (i.e., within 10 degrees) along a primary substrate surface and may be relative to which the substrate is processed during fabrication, and vertical is a direction generally orthogonal thereto. Reference to “exactly horizontal” is the direction along the primary substrate surface (i.e., no degrees there-from) and may be relative to which the substrate is processed during fabrication. Further, “vertical” and “horizontal” as used herein are generally perpendicular directions relative one another and independent of orientation of the substrate in three-dimensional space. Additionally, “elevationally-extending” and “extend(ing) elevationally” refer to a direction that is angled away by at least 45° from exactly horizontal. Further, “extend(ing) elevationally”, “elevationally-extending”, “extend(ing) horizontally”, “horizontally-extending” and the like with respect to a field effect transistor are with reference to orientation of the transistor’s channel length along which current flows in operation between the source/drain regions. For bipolar junction transistors, “extend(ing) elevationally” “elevationally-extending”, “extend(ing) horizontally”, “horizontally-extending” and the like, are with reference to orientation of the base length along which current flows in operation between the emitter and collector. In some embodiments, any component, feature, and/or region that extends elevationally extends vertically or within 10° of vertical.

Further, “directly above”, “directly below”, and “directly under” require at least some lateral overlap (i.e., horizontally) of two stated regions/materials/components relative one another. Also, use of “above” not preceded by “directly” only requires that some portion of the stated region/material/component that is above the other be elevationally outward of the other (i.e., independent of whether there is any lateral overlap of the two stated regions/materials/components). Analogously, use of “below” and “under” not preceded by “directly” only requires that some portion of the stated region/material/component that is below/under the other be elevationally inward of the other (i.e., independent of whether there is any lateral overlap of the two stated regions/materials/components).

Any of the materials, regions, and structures described herein may be homogenous or non-homogenous, and regardless may be continuous or discontinuous over any material which such overlie. Where one or more

example composition(s) is/are provided for any material, that material may comprise, consist essentially of, or consist of such one or more composition(s). Further, unless otherwise stated, each material may be formed using any suitable existing or future-developed technique, with
5 atomic layer deposition, chemical vapor deposition, physical vapor deposition, epitaxial growth, diffusion doping, and ion implanting being examples.

Additionally, “thickness” by itself (no preceding directional adjective) is defined as the mean straight-line distance through a given material or
10 region perpendicularly from a closest surface of an immediately-adjacent material of different composition or of an immediately-adjacent region. Additionally, the various materials or regions described herein may be of substantially constant thickness or of variable thicknesses. If of variable thickness, thickness refers to average thickness unless otherwise indicated,
15 and such material or region will have some minimum thickness and some maximum thickness due to the thickness being variable. As used herein, “different composition” only requires those portions of two stated materials or regions that may be directly against one another to be chemically and/or physically different, for example if such materials or regions are not
20 homogenous. If the two stated materials or regions are not directly against one another, “different composition” only requires that those portions of the two stated materials or regions that are closest to one another be chemically and/or physically different if such materials or regions are not homogenous. In this document, a material, region, or structure is “directly against”
25 another when there is at least some physical touching contact of the stated materials, regions, or structures relative one another. In contrast, “over”, “on”, “adjacent”, “along”, and “against” not preceded by “directly” encompass “directly against” as well as construction where intervening material(s), region(s), or structure(s) result(s) in no physical touching
30 contact of the stated materials, regions, or structures relative one another.

Herein, regions-materials-components are “electrically coupled” relative one another if in normal operation electric current is capable of continuously flowing from one to the other and does so predominately by movement of subatomic positive and/or negative charges when such are
35 sufficiently generated. Another electronic component may be between and

electrically coupled to the regions-materials-components. In contrast, when regions-materials-components are referred to as being "directly electrically coupled", no intervening electronic component (e.g., no diode, transistor, resistor, transducer, switch, fuse, etc.) is between the directly electrically
5 coupled regions-materials-components.

The composition of any of the conductive/conductor/conducting materials herein may be metal material and/or conductively-doped semiconductive/semiconductor/semiconducting material. "Metal material" is any one or combination of an elemental metal, any mixture or alloy of two
10 or more elemental metals, and any one or more conductive metal compound(s).

Herein, "selective" as to etch, etching, removing, removal, depositing, forming, and/or formation is such an act of one stated material relative to another stated material(s) so acted upon at a rate of at least 2:1 by volume.
15 Further, selectively depositing, selectively growing, or selectively forming is depositing, growing, or forming one material relative to another stated material or materials at a rate of at least 2:1 by volume for at least the first 75 Angstroms of depositing, growing, or forming.

Unless otherwise indicated, use of "or" herein encompasses either and
20 both.

CONCLUSION

In some embodiments, a method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs)
25 comprises forming a stack comprising vertically-alternating insulative tiers and conductive tiers. The stack comprises a TAV region and an operative memory-cell-string region. The TAV region comprises spaced operative TAV areas. Operative channel-material strings are formed in the stack in the operative memory-cell-string region and dummy channel-material strings are
30 formed in the stack in the TAV region laterally outside of and not within the operative TAV areas. Operative TAVs are formed in individual of the spaced operative TAV areas in the TAV region.

In some embodiments, a method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs)
35 comprises forming a stack comprising vertically-alternating insulative tiers

and conductive tiers. The insulative tiers comprise insulative first material. The conductive tiers comprise a second material of different composition from that of the first material. The stack comprises a TAV region and an operative memory-cell-string region. Operative channel-material strings are
5 formed in the stack in the operative memory-cell-string region and dummy channel-material strings are formed in the stack in the TAV region. Operative TAVs are formed in the TAV region. Horizontally-elongated trenches are formed into the stack. The second material from the conductive tiers is replaced with conducting material that is used to form individual
10 conductive lines in the conductive tiers. Elevationally-extending strings of memory cells are formed in the stack. Individual of the memory cells comprise channel material of the operative channel-material strings, a gate region that is part of one of the individual conductive lines, and a memory structure laterally between the gate region and the channel material of the
15 operative channel-material strings in the individual conductive tiers.

In some embodiments, a method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs) comprises forming a stack comprising vertically-alternating insulative tiers and conductive tiers with the stack comprising an operative
20 memory-cell-string region. The stack comprises a stair-step region comprising a landing region comprising a TAV region. Operative channel-material strings are formed in the stack in the operative memory-cell-string region and dummy channel-material strings in the stack in the TAV region of the landing region. Operative TAVs are formed in the
25 TAV region of the landing region. An operative stair-step structure is formed into the stack in the stair-step region and a landing in the landing region of the stair-step region.

In some embodiments, a memory array comprises a vertical stack comprising alternating insulative tiers and conductive tiers. The conductive
30 tiers comprise gate regions of individual memory cells. The gate regions individually comprise part of a conductive line in individual of the conductive tiers. Operative channel-material strings extend through the insulative tiers and the conductive tiers. The individual memory cells comprise a memory structure laterally between individual of the gate regions
35 and channel material of the operative channel-material strings. An operative

stair-step structure comprises the insulative tiers and the conductive tiers. A landing region is adjacent the steps of the operative stair-step structure. The landing region comprises a landing and operative TAVs extending through the insulative tiers and the conductive tiers. The landing region comprises

5 dummy channel-material strings in the insulative tiers and the conductive tiers.

CLAIMS:

1. A method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs), the method comprising:
 - 5 forming a stack comprising vertically-alternating insulative tiers and conductive tiers, the stack comprising a TAV region and an operative memory-cell-string region, the TAV region comprising spaced operative TAV areas;
 - forming operative channel-material strings in the stack in the
 - 10 operative memory-cell-string region and forming dummy channel-material strings in the stack in the TAV region laterally outside of and not within the operative TAV areas; and
 - forming operative TAVs in individual of the spaced operative TAV areas in the TAV region.
- 15 2. The method of claim 1 comprising forming the operative and dummy channel-material strings at the same time.
3. The method of claim 1 comprising forming the operative TAVs after forming the operative and dummy channel-material strings.
4. The method of claim 1 comprising forming the operative and
- 20 dummy channel-material strings to individually have the same horizontal shape relative one another.
5. The method of claim 1 comprising forming the operative and dummy channel-material strings to individually have the same size and shape relative one another.
- 25 6. The method of claim 1 comprising forming the operative channel-material strings and the dummy channel-material strings to have the same pitch relative one another.
7. The method of claim 6 comprising forming the operative and
- 30 dummy channel-material strings to individually have the same size and shape relative one another.

8. The method of claim 1 comprising forming the operative and dummy channel-material strings to individually be horizontally smaller than the operative TAVs.

9. The method of claim 1 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane; the dummy channel-material strings, the TAV region, and the operative TAVs being within the memory plane.

10. The method of claim 1 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane; the dummy channel-material strings, the TAV region, and the operative TAVs being outside of the memory plane.

11. The method of claim 10 wherein the dummy channel-material strings, the TAV region, and the operative TAVs are edge-of-plane.

12. The method of claim 10, wherein the dummy channel-material strings, the TAV region, and the operative TAVs are formed in a landing region of a stair-step region; and further comprising:

forming an operative stair-step structure into the stack in the stair-step region and a landing in the landing region of the stair-step region.

13. The method of claim 12 wherein the landing is a crest of the operative stair-step structure.

14. The method of claim 1 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane; and further comprising:

forming multiple of said TAV regions that are laterally spaced relative one another, at least one of said TAV regions being within the memory plane, at least another one of said TAV regions being outside of the memory plane.

15. The method of claim 1 comprising forming CMOS-under-array circuitry.

16. The method of claim 1 wherein the operative TAVs directly electrically couple digitlines of the memory array with CMOS-under-array
5 circuitry.

17. The method of claim 1 comprising forming the memory array to comprise NAND.

18. The method of claim 1 comprising:
forming individual memory cells of the strings of memory cells to
10 comprise channel material of the operative channel-material strings, a gate region that is part of a conductive line in individual of the conductive tiers, and a memory structure laterally between the gate region and the channel material of the operative channel-material strings in the individual conductive tiers; and
15 forming conducting material of the conductive lines after forming the operative and dummy channel-material strings.

19. The method of claim 1 comprising:
forming individual memory cells of the strings of memory cells to
comprise channel material of the operative channel-material strings, a gate
20 region that is part of a conductive line in individual of the conductive tiers, and a memory structure laterally between the gate region and the channel material of the operative channel-material strings in the individual conductive tiers; and
forming conducting material of the conductive lines before forming
25 the operative and dummy channel-material strings.

20. A method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs), the method comprising:

5 forming a stack comprising vertically-alternating insulative tiers and conductive tiers, the insulative tiers comprising insulative first material, the conductive tiers comprising a second material of different composition from that of the first material, the stack comprising a TAV region and an operative memory-cell-string region;

10 forming operative channel-material strings in the stack in the operative memory-cell-string region and forming dummy channel-material strings in the stack in the TAV region;

forming operative TAVs in the TAV region;

forming horizontally-elongated trenches into the stack;

15 replacing the second material from the conductive tiers with conducting material that is used to form individual conductive lines in the conductive tiers; and

20 forming elevationally-extending strings of memory cells in the stack; individual of the memory cells comprising channel material of the operative channel-material strings, a gate region that is part of one of the individual conductive lines, and a memory structure laterally between the gate region and the channel material of the operative channel-material strings in the individual conductive tiers.

21. The method of claim 20 comprising forming the operative channel-material strings and the dummy channel-material strings to have the same pitch relative one another.

22. The method of claim 21 comprising forming the operative and dummy channel-material strings to individually have the same size and shape relative one another.

23. The method of claim 20 wherein the operative channel-material strings are within laterally-spaced memory blocks that comprise part of a memory plane.

24. The method of claim 20 wherein the TAV region comprises spaced operative TAV areas, the dummy channel-material strings are formed laterally outside of and not within the operative TAV areas, and the operative TAVs are formed in individual of the spaced operative TAV areas
5 of the TAV region.

25. A method used in forming a memory array comprising strings of memory cells and operative through-array-vias (TAVs), the method comprising:

forming a stack comprising vertically-alternating insulative tiers and
10 conductive tiers, the stack comprising an operative memory-cell-string region, the stack comprising a stair-step region comprising a landing region comprising a TAV region;

forming operative channel-material strings in the stack in the operative memory-cell-string region and dummy channel-material strings in
15 the stack in the TAV region of the landing region;

forming operative TAVs in the TAV region of the landing region; and
forming an operative stair-step structure into the stack in the stair-step region and a landing in the landing region of the stair-step region.

26. The method of claim 25 comprising forming the operative stair-
20 step structure and the landing before forming the operative TAVs.

27. The method of claim 25 comprising forming the operative and dummy channel-material strings before forming the operative stair-step structure and the landing.

28. The method of claim 27 comprising forming the operative stair-
25 step structure and the landing before forming the operative TAVs.

29. The method of claim 25 wherein the landing is a crest of the operative stair-step structure.

30. A memory array comprising:
- a vertical stack comprising alternating insulative tiers and conductive tiers, the conductive tiers comprising gate regions of individual memory cells, the gate regions individually comprising part of a conductive line in individual of the conductive tiers; operative channel-material strings extending through the insulative tiers and the conductive tiers;
- the individual memory cells comprising a memory structure laterally between individual of the gate regions and channel material of the operative channel-material strings;
- an operative stair-step structure comprising the insulative tiers and the conductive tiers; and
- a landing region adjacent steps of the operative stair-step structure, the landing region comprising a landing and operative TAVs extending through the insulative tiers and the conductive tiers, the landing region comprising dummy channel-material strings in the insulative tiers and the conductive tiers.

31. The memory array of claim 30 wherein the operative and dummy channel-material strings individually have the same horizontal shape relative one another.

32. The memory array of claim 30 wherein the operative and dummy channel-material strings individually have the same size and shape relative one another.

33. The memory array of claim 30 wherein the operative channel-material strings and the dummy channel-material strings have the same pitch relative one another.

34. The memory array of claim 33 wherein the operative and dummy channel-material strings individually have the same size and shape relative one another.

35. The memory array of claim 30 wherein the operative and dummy channel-material strings individually are horizontally smaller than the operative TAVs.

36. The memory array of claim 30 comprising CMOS-under-array circuitry.

37. The memory array of claim 30 comprising NAND.