WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a substrate having a memory cell region, a peripheral region, and a dam region between the memory cell region and the peripheral region, the memory cell region having a rectangular shape according to a top view and having a plurality of active regions defined therein;

a plurality of bit line structures extending on the substrate in the memory cell region to be parallel with each other in a first horizontal direction, each bit line structure including a bit line;

a plurality of buried contacts filling lower portions of spaces among the plurality of bit line structures on the substrate;

a plurality of landing pads on the plurality of buried contacts; and

a dam structure including a first dam structure and a second dam structure in the dam region and being at the same level as the plurality of landing pads,

wherein the first dam structure has a line shape extending in the first horizontal direction,

wherein the second dam structure is separated from the first dam structure with a first dam opening between the first dam structure and the second dam structure and has a line shape extending in a second horizontal direction that is perpendicular to the first horizontal direction,

wherein the plurality of buried contacts includes a plurality of first dummy buried contacts and a plurality of second dummy buried contacts,

wherein each of the plurality of first dummy buried contacts has a top surface contacting a bottom surface of the first dam structure,

wherein each of the plurality of second dummy buried contacts has a top surface contacting a bottom surface of the second dam structure,

wherein the plurality of first dummy buried contacts are electrically separated from the plurality of active regions, and

wherein the plurality of second dummy buried contacts are in contact with the plurality of active region.

2. The semiconductor memory device of claim 1, wherein opposite sides of a top surface of the first dam structure extend in straight lines in the first horizontal direction and opposite sides of a top surface of the second dam structure extend in straight lines in the second horizontal direction, the opposite sides respectively facing the memory cell region and the peripheral region.

3. The semiconductor memory device of claim 1 or claim 2, wherein each of the plurality of landing pads has a top surface having a disc shape, and

wherein the plurality of landing pads are arranged to zigzag in the first horizontal direction or the second horizontal direction in a honeycomb pattern.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the first dam structure is arranged along a side of the rectangular shape of the memory cell region, the side of the rectangular shape extending in the first horizontal direction, and

wherein the second dam structure is arranged along a side of the rectangular shape of the memory cell region, the side of the rectangular shape extending in the second horizontal direction.

5. The semiconductor memory device of any one of claims 1 to 4, wherein each of the first dam structure and the second dam structure has a plurality of portions separated from each other by a second dam opening,

wherein the plurality of portions of the first dam structure is sequentially arranged in the first horizontal direction, and

wherein the plurality of portions of the second dam structure is sequentially arranged in the second horizontal direction.

6. The semiconductor memory device of claim 5, wherein each of the first dam opening and the second dam opening has a width of about 1 um to about 5 um.

7. The semiconductor memory device of claim 1, further comprising:

a dummy bit line structure extending on the substrate in the second horizontal direction,

wherein the second dam structure extends from top surfaces of the plurality of second dummy buried contacts to a top surface of the dummy bit line structure.

8. The semiconductor memory device of claim 7, wherein, in the first horizontal direction, a width of the dummy bit line structure is greater than a width of each of the plurality of bit line structures.

9. The semiconductor memory device of any one of claims 1 to 8, further comprising:

a plurality of capacitor structures formed in the memory cell region,

wherein the plurality of capacitor structures are formed by an upper electrode, a

plurality of lower electrodes electrically connected to the plurality of landing pads, and a capacitor dielectric film between the upper electrode and a plurality of lower electrodes, and

wherein the dam structure is not electrically connected to the plurality of landing pads.

10. A semiconductor memory device comprising:

a substrate having a memory cell region, a peripheral region, and a dam region between the memory cell region and the peripheral region, the memory cell region having a rectangular shape according to a top view and having a plurality of active regions defined therein;

a plurality of bit line structures extending on the substrate in the memory cell region to be parallel with each other in a first horizontal direction, each bit line structure including a bit line;

a plurality of gate line structures in the peripheral region, each of the plurality of gate line structures having a gate line pattern at the same level as the bit line;

a buried contact filling a lower portion of a space between the plurality of bit line structures on the substrate;

a landing pad on the buried contact; and

a dam structure arranged along sides of the rectangular shape of the memory cell region in the dam region, wherein the top surface of the dam structure is at the same level as a top surface of the landing pad, and wherein a bottom surface of the dam structure is at the same level as a bottom surface of the landing pad,

wherein a side of a top surface of the dam structure extends in a straight line and faces the memory cell region,

wherein the buried contact includes a first dummy buried contact and a second

dummy buried contact,

wherein each of the first dummy buried contact and the second dummy buried contact has a top surface contacting a bottom surface of the dam structure,

wherein the first dummy buried contact is electrically separated from the plurality of active regions, and

wherein the second dummy buried contact is in contact with at least one of the plurality of active regions.

11. The semiconductor memory device of claim 10, wherein, according to the top view, the dam structure has a rectangular shape surrounding the memory cell region.

12. The semiconductor memory device of claim 10 or claim 11, wherein the dam structure extends along four sides of the rectangular shape of the memory cell region and is separated into a plurality of portions at each corner of the rectangular shape of the memory cell region.

13. The semiconductor memory device of claim 12, wherein the dam structure includes at least two portions sequentially arranged and separated from each other along at least one of the four sides of the rectangular shape of the memory cell region.

14. The semiconductor memory device of any one of claims 10 to 13, further comprising:

a plurality of capacitor structures formed in the memory cell region,

wherein the plurality of capacitor structures are formed by an upper electrode, a plurality of lower electrodes, and a capacitor dielectric film between the upper electrode and

a plurality of lower electrodes, a corresponding lower electrode electrically connected to the landing pad, and

wherein the dam structure is not electrically connected to the landing pad.

15. The semiconductor memory device of any one of claims 10 to 14, wherein the landing pad and the dam structure are formed of the same material.

16. A semiconductor memory device comprising:

a substrate having a memory cell region, a peripheral region, and a dam region between the memory cell region and the peripheral region, the memory cell region having a rectangular shape according to a top view and having a plurality of active regions defined therein;

a plurality of word lines extending across the plurality of active regions in the memory cell region in a first horizontal direction, the plurality of word lines being parallel with each other;

a plurality of bit line structures extending on the substrate in the memory cell region to be parallel with each other in a second horizontal direction that is perpendicular to the first horizontal direction, each bit line structure including a bit line;

a plurality of gate line structures in the peripheral region, each of the plurality of gate line structures having a gate line pattern at the same level as the bit line in a vertical direction;

a plurality of buried contacts filling lower portions of spaces among the plurality of bit line structures on the substrate;

a plurality of landing pads filling upper portions of the spaces among the plurality of bit line structures and extending over the plurality of bit line structures; and

a dam structure including a first dam structure and a second dam structure in the dam

region and being at the same level as the plurality of landing pads in the vertical direction,

wherein the first dam structure has a line shape extending in the first horizontal direction,

wherein the second dam structure has a line shape extending in the second horizontal direction,

wherein the first dam structure and the second dam structure are separated from each other by a first dam opening at a corner of the rectangular shape of the memory cell region,

wherein each of the plurality of landing pads has a top surface having a disc shape,

wherein opposite sides of a top surface of the first dam structure extend in straight lines in the first horizontal direction,

wherein opposite sides of a top surface of the second dam structure extend in straight lines in the second horizontal direction,

wherein the opposite sides respectively face the memory cell region and the peripheral region,

wherein the plurality of buried contacts includes a plurality of first dummy buried contacts and a plurality of second dummy buried contacts,

wherein each of the plurality of first dummy buried contacts has a top surface contacting a bottom surface of the first dam structure,

wherein each of the plurality of second dummy buried contacts has a top surface contacting a bottom surface of the second dam structure,

wherein the plurality of first dummy buried contacts are electrically separated from the plurality of active regions, and

wherein the plurality of second dummy buried contacts are in contact with the plurality of active region.

17. The semiconductor memory device of claim 16, wherein at least one selected from the first dam structure and the second dam structure includes a plurality of portions separated from each other by a second dam opening along at least one side of the rectangular shape of the memory cell region.

18. The semiconductor memory device of claim 16 or claim 17, wherein the plurality of first dummy buried contacts having the top surface contacting the bottom surface of the first dam structure among the plurality of buried contacts are electrically separated from the plurality of active regions with an insulating film pattern between the plurality of first dummy buried contacts and the plurality of active regions.