PCRAM ARRAY STACK

[0001] This application is a continuation-in-part of U.S. Patent Application No. 10/120,521 filed April 12, 2002, which is a continuation of U.S. Patent Application No. 10/077,867 filed February 2, 2002, the contents of both being incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material.

BACKGROUND

[0003] Recently resistance variable memory elements, which include Programmable Conductive Random Access Memory (PCRAM) elements, have been investigated for suitability as semi-volatile and non-volatile random access memory devices. A typical PCRAM device is disclosed in U.S. Patent No. 6,348,365 to Moore and Gilton. In typical PCRAM devices, conductive material, such as silver, is incorporated into a chalcogenide material. The resistance of the chalcogenide material can be programmed to stable higher resistance and lower resistance states. The unprogrammed PCRAM device is normally in a high resistance state. A write operation programs the PCRAM device to a lower resistance state by applying a voltage potential across the chalcogenide material.

[0004] The programmed lower resistance state can remain intact for an indefinite period, typically ranging from hours to weeks, after the voltage potentials are removed. The PCRAM device can be returned to its higher resistance state by applying a reverse voltage potential of about the same order of magnitude as used to write the element to the lower resistance state. Again, the higher resistance state is maintained in a semi-volatile manner once the voltage potential is removed. In this

way, such a device can function as a resistance variable memory element having two resistance states, which can define two logic states.

[0005] A PCRAM device can incorporate a chalcogenide glass comprising germanium selenide (Ge_xSe_{100-x}). The germanium selenide glass may also incorporate silver (Ag) or silver selenide (Ag_2Se).

[0006] The amorphous nature of the chalcogenide glass material used in a PCRAM device has a direct bearing on its programming characteristics. Thus, incorporation of silver into the chalcogenide glass requires precise control of the glass composition and silver concentration so as not to cause the chalcogenide glass to change from the desired amorphous state to a crystalline state.

[0007] Accordingly, there is a need for a resistance variable memory element having improved memory retention and switching characteristics.

BRIEF SUMMARY OF THE INVENTION

[0008] The invention provides a resistance variable memory element and a method of forming a resistance variable memory element.

[0009] In one embodiment, the invention provides a memory element having at least one layer of silver-selenide between a first chalcogenide glass layer and a conductive adhesive layer. The conductive adhesive layer may also be a chalcogenide glass layer. The stack of layers comprising a first chalcogenide glass layer, a silver-selenide layer, and a second chalcogenide glass layer are formed between two conductive layers or electrodes. In another embodiment of the invention, the stack of layers may contain more than one silver-selenide layer between the chalcogenide glass layer and the conductive adhesion layer. In another embodiment, the memory element may contain layers of chalcogenide glass, layers of silver, and layers of silver-selenide, in various orders, between the electrodes. The invention provides structures for PCRAM devices with improved memory characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The above-discussed and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

[0011] FIGS. 1-7 illustrate cross-sectional views of a memory element fabricated in accordance with an embodiment of the invention and at different stages of processing.

[0012] FIG. 8 illustrates a cross-sectional view of a memory element as shown in FIG. 1 at a stage of processing subsequent to that shown in FIG. 4.

[0013] FIG. 9 illustrates a cross-sectional view of a memory element in accordance with an embodiment of the invention at a stage of processing subsequent to that shown in FIG. 4.

[0014] FIG. 10 illustrates a cross-sectional view of a memory element in accordance with an embodiment of the invention at a stage of processing subsequent to that shown in FIG. 4.

[0015] FIG. 11 illustrates a cross-sectional view of a memory element in accordance with an embodiment of the invention.

[0016] FIG. 12 illustrates a cross-sectional view of a memory element in accordance with another embodiment of the invention.

[0017] FIG. 13 illustrates a cross-sectional view of a memory element in accordance with another embodiment of the invention.

[0018] FIG. 14 illustrates a cross-sectional view of a memory element in accordance with another embodiment of the invention.

[0019] FIG. 15 illustrates a computer system having a memory element in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0021] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation. The substrate need not be semiconductor-based, but may be any support structure suitable for supporting an integrated circuit.

[0022] The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is conductive, and as long as the physical and electrical properties of the silver remain unchanged.

[0023] The term "silver-selenide" is intended to include various species of silver-selenide, including some species which have a slight excess or deficit of silver. For example, silver-selenide species may be represented by the general formula $Ag_{2\ +/-x}Se$. Though not being limited by a particular stoichiometric ratio between Ag and Se, devices of the present invention typically comprise an $Ag_{2\ +/-x}Se$ species where x ranges from about 1 to about 0.

[0024] The term "semi-volatile memory" is intended to include any memory device or element which is capable of maintaining its memory state after power is removed from the device for some period of time. Thus, semi-volatile memory devices are capable of retaining stored data after the power source is disconnected or removed. Accordingly, the term "semi-volatile memory" is also intended to include not only semi-volatile memory devices, but also non-volatile memory devices and those of low volatility.

[0025] The term "resistance variable material" is intended to include chalcogenide glasses, and chalcogenide glasses comprising a metal, such as silver or metal ions. For instance, the term "resistance variable material" may include silver doped chalcogenide glasses, silver-germanium-selenide glasses, chalcogenide glass comprising a silver selenide layer, and non-doped chalcogenide glass.

[0026] The term "resistance variable memory element" is intended to include any memory element, including Programmable Conductor Random Access Memory elements, which exhibit a resistance change in response to an applied voltage.

[0027] The term "chalcogenide glass" is intended to include glasses that comprise an element from group VIA (or group 16) of the periodic table. Group VIA elements, also referred to as chalcogens, include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O).

[0028] The invention will now be explained with reference to the figures, which illustrate exemplary embodiments and where like reference numbers indicate like features. FIG. 1 depicts a portion of an optional insulating layer 12 formed over a semiconductor substrate 10, for example, a silicon substrate. It should be understood that the memory elements of the invention can be formed over a variety of substrate materials and not just semiconductor substrates such as silicon, as shown above. For example, the optional insulating layer 12 may be formed on a ceramic or

polymer-based substrate. The insulating layer 12 may be formed by any known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The insulating layer 12 may be formed of a conventional insulating oxide, such as silicon oxide (SiO_2), a silicon nitride (Si_3N_4), or a low dielectric constant material, among many others.

[0029] A first electrode 14 is formed over the insulating layer 12, as also illustrated in FIG. 1. The first electrode 14 may comprise any conductive material, for example, tungsten, nickel, tantalum, aluminum, platinum, conductive nitrides, and other materials. A second insulating layer 15 is next formed over the first electrode 14. The second insulating layer 15 may comprise the same or different materials as those described above with reference to the insulating layer 12.

[0030] Referring now to FIG. 2, an opening 13 extending to the first electrode 14 is formed in the second insulating layer 15. The opening 13 may be formed by known methods in the art, for example, by a conventional patterning and etching process. A first chalcogenide glass layer 17 is next formed over the second insulating layer 15, to fill in the opening 13, as shown in FIG. 3.

[0031] According to an embodiment of the invention, the first chalcogenide glass layer 17 can be germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry. The preferred stoichiometric range is between about $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$ and is more preferably about $Ge_{40}Se_{60}$. The first chalcogenide glass layer 17 preferably has a thickness from about 100 Å to about 1000 Å and is more preferably about 150 Å.

[0032] The formation of the first chalcogenide glass layer 17, having a stoichiometric composition in accordance with the invention, may be accomplished by any suitable method. For instance, germanium-selenide glass can be formed by evaporation, co-sputtering germanium and selenium in the appropriate ratios, sputtering using a germanium-selenide target having the desired stoichiometry, or

chemical vapor deposition with stoichiometric amounts of GeH_4 and SeH_2 gases (or various compositions of these gases), which result in a germanium-selenide film of the desired stoichiometry, are examples of methods which may be used.

[0033] As shown in FIG. 4, metal containing layer 18 may be directly deposited on the surface of the first chalcogenide glass layer, 17. When a metal containing layer 17, such as a silver-selenide layer, is provided in contact with the chalcogenide glass, doping the chalcogenide glass layer 17 by photodoping or thermal diffusion becomes unnecessary. However, doping the chalcogenide glass layer 17 with a metal (e.g. silver) is an optional variant.

[0034] The metal containing layer 18 may be any suitable metal containing layer. For instance, suitable metal containing layers include silver-chalcogenide layers, such as silver-sulfide, silver-oxide, silver-telluride, and silver-selenide. A variety of processes can be used to form the preferred metal containing layer 18, which is silver-selenide. For instance, physical vapor deposition techniques such as evaporative deposition and sputtering may be used. Other processes such as chemical vapor deposition, co-evaporation or depositing a layer of selenium above a layer of silver to form a silver-selenide layer can also be used.

[0035] Preferably, the thickness of the metal containing layers 17, 18 can be such that a ratio of the metal containing layer 18 to the first chalcogenide glass layer 17 thicknesses is between about 5:1 and about 1:1. In other words, the thickness of the metal containing layer 18 is between about 1 to about 5 times greater than the thickness of the first chalcogenide glass layer 17. Even more preferably, the ratio is between about 3.1:1 and about 2:1.

[0036] Referring now to FIG. 5, a second glass layer 20 can be formed over the first metal containing layer 18. Where the metal containing layer is silver-selenide, the second glass layer 20 allows deposition of silver above the silver-selenide layer, while preventing agglomeration of silver on the surface of the silver-

selenide . The second glass layer 20 may prevent or regulate migration of metal, such as silver, from an electrode 22 (FIG. 6) into the memory element.

[0037] The second glass layer 20 may also act as a silver diffusion control layer or an adhesion layer. For use as a diffusion control layer, any suitable glass may be used, including but not limited to chalcogenide glasses. The second chalcogenide glass layer 20 may, but need not, have the same stoichiometric composition as the first chalcogenide glass layer, e.g., Ge_xSe_{100-x}. Thus, the second glass layer 20 may be of a different material, different stoichiometry, and/or more rigid than the first chalcogenide glass layer 17. When used as a diffusion control layer, the second glass layer 20 may comprise SiSe (silicon-selenide), AsSe (arsenic-selenide, such as As_3Se_2), GeS (germanium-sulfide), and combinations of Ge, Ag, and Se. Any one of these suitable glass materials may further comprise small concentrations, e.g. less than about 3%, of dopants to include nitrides, metal, and other group 13-16 elements from the periodic table.

[0038] The thickness of the layers 18, 20 are such that the metal containing layer 18 thickness is greater than the thickness of the second glass layer 20. Preferably, a ratio of the metal containing layer 18 thickness to the second glass layer 20 thickness is between about 5:1 and about 1:1. More preferably, the ratio of the metal containing layer 18 thickness to the thickness of the second glass layer 20 is between about 3.3:1 and about 2:1. The second glass layer 20 preferably has a thickness between about 100 Å to about 1000 Å and is more preferably about 150 Å. The second glass layer 20 may be formed by any suitable method. For example, chemical vapor deposition, evaporation, co-sputtering, or sputtering using a target having the desired stoichiometry, may be used.

[0039] Referring now to FIG. 6, a second conductive electrode 22 is formed over the second glass layer 20. The second conductive electrode 22 may comprise any electrically conductive material, for example, tungsten, tantalum, titanium, conductive nitrides, or other materials. Thus, advantageously, the second

glass layer 20 may be chosen to considerably slow or prevent migration of electrically conductive metals, such as silver, through the resistance variable memory element 100.

[0040] Referring now to FIG. 7, one or more additional insulating layers 30 may be formed over the second electrode 22 and the second insulating layer 15 to isolate the resistance variable memory element 100 from other structures fabricated over the substrate 10. Conventional processing steps can then be carried out to electrically couple the resistance variable memory element to various circuits of a memory array.

[0041] In accordance with another embodiment of the invention, one or more layers of a metal containing material, such as silver-selenide, may be deposited over the first chalcogenide glass layer 17. A plurality of metal containing layers may be used. As shown in FIG. 8, an optional second silver-selenide layer 19 may be deposited on the first silver-selenide layer 18 subsequent to the processing step, which results in the structure shown in FIG. 4.

[0042] The thickness of the metal containing layers 18, 19 is such that the total thickness of these combined layers, e.g. silver-selenide layers, is greater than or equal to the thickness of the first chalcogenide glass layer 17. The total thickness of the combined metal containing layers 18, 19 is also greater than the thickness of a second glass layer 20. It is preferred that the total thickness of the combined metal containing layers 18, 19 is between about 1 to about 5 times greater than the thickness of the first chalcogenide glass layer 17 and accordingly between about 1 to about 5 times greater than the thickness of the second glass layer 20. It is even more preferred that the total thickness of the combined metal containing layers 18, 19 is between about 2 to about 3.3 times greater than the thicknesses of the first chalcogenide glass layer 17 and the second glass layer 20.

[0043] In accordance, with another embodiment of the invention, the first chalcogenide glass layer 17 may comprise a plurality of layers of a chalcogenide glass material, such as germanium-selenide. The second glass layer 20 may also comprise a plurality of layers of a glass material. Any suitable number of layers may be used to comprise the first chalcogenide glass layer 17 and/or the second glass layer 20. However it is to be understood that the total thickness of the metal containing layer(s) 18,19 should be thicker than the total thickness of the plurality of chalcogenide glass layers 17 and additionally the total thickness of the metal containing layer(s) 18, 19 should be thicker than the total thickness of the one or more layers of the second glass layer 20. Preferably a ratio of the total thickness of the metal containing layer(s) 18, 19 to the total thickness of the plurality of layers of chalcogenide glass 17 is between about 5:1 and about 1:1. Also, preferably a ratio of the total thickness of the metal containing layer(s) 18, 19 to the total thickness of the plurality of layers of the second glass layer 20 is between about 5:1 and about 1:1.

[0044] Referring now to FIG. 7, in accordance with another embodiment of the invention, one or more of the chalcogenide glass layers 17, 20 may also be doped with a dopant, such as a metal, preferably silver.

[0045] In accordance with another embodiment of the invention as illustrated in FIG. 9, which shows a stage of processing subsequent to that shown in FIG. 4, the stack of layers formed between the first and second electrodes may include alternating layers of chalcogenide glass 17, 117, 217, 317 and metal containing layers 18, 118, 218. A desirable metal containing layer is silver-selenide. As shown in FIG. 9, a first chalcogenide glass layer 17 is positioned over a first electrode 14, a first silver-selenide layer 18 is positioned over the first chalcogenide glass layer 17, a second chalcogenide glass layer 117 is positioned over the first silver-selenide layer 18, a second silver-selenide layer 118 is positioned over the second chalcogenide glass layer 117, a third chalcogenide glass layer 217 is

positioned over the second silver-selenide layer 118, a third silver-selenide layer 218 is positioned over the third chalcogenide glass layer 217, and a fourth chalcogenide glass layer 317 is positioned over the third silver-selenide layer 218. The second conductive electrode 22 can be formed over the fourth chalcogenide glass layer 317.

[0046] In accordance with this same embodiment, the memory element 100 comprises at least two metal containing layers 18, 118 and at least three chalcogenide glass layers 17, 117, 217. However, it is to be understood that the memory element 100 may comprise a plurality of alternating layers of chalcogenide glass 17, 117, 217 and silver-selenide 18, 118, so long as the alternating layers start with a first chalcogenide glass layer, e.g 17, and end with a last chalcogenide glass layer, e.g. 317, with the first chalcogenide glass layer contacting a first electrode 14 and the last chalcogenide glass layer contacting a second electrode 22. The thickness and ratios of the alternating layers of silver-selenide 18, 118, 218 and chalcogenide glass 17, 117, 217, 317 are the same as described above, in that the silver-selenide layers 18, 118, 218 are preferably thicker than connecting chalcogenide glass layers 17, 117, 217, 317 in a ratio of between about 5:1 and about 1:1 silver-selenide layer 18, 118, 218 to connected chalcogenide glass layer 17, 117, 217, 317, and more preferably between about 3.3:1 and 2:1 silver-selenide layer 18, 118, 218 to connected chalcogenide glass layer 17, 117, 217, 317.

[0047] As shown in FIG. 10, in another embodiment of the invention, one or more layers of a metal containing material 18, 418, such as silver-selenide, may be deposited between the chalcogenide glass layers 17, 117. A plurality of silver-selenide layers 18, 418 may be used. Thus, as shown in FIG. 10, at a processing step subsequent to that shown in FIG. 4, an additional silver-selenide layer 418 may be deposited on the first silver-selenide layer 18 and an additional silver-selenide layer 518 may be deposited on the third silver-selenide layer 218.

[0048] In accordance with another embodiment of the invention, each of the chalcogenide glass layers 17, 117, 217, 317 shown in FIG. 10 may comprise a

plurality of thinner layers of a chalcogenide glass material, such as germanium-selenide. Any suitable number of layers may be used to comprise the chalcogenide glass layers 17, 117, 217, 317.

[0049] In another embodiment of the invention, one or more of the chalcogenide glass layers 17, 117, 217, 317 may also be doped with a dopant such as a metal, which is preferably silver. It should be noted that when a chalcogenide glass layer, such as layer 117, is sputter deposited over a silver selenide layer, such as layer 418, the energetic nature of the sputtering process may cause a small amount of Ag to be incorporated into the chalcogenide glass layer.

[0050] Devices constructed according to the embodiments of the invention, particularly those having a silver-selenide layer (e.g. layer 18) disposed between two chalcogenide glass layers (e.g. layers 17, 20) show improved memory retention and write/erase performance over conventional memory devices. These devices have also shown data retention for more than 1200 hours at room temperature. The devices switch at pulse widths less than 2 nanoseconds compared with doped resistance variable memory elements of the prior art that switch at about 100 nanosecond pulses.

[0051] As shown in FIG. 11, in accordance with another embodiment of the present invention and similar to the first exemplary embodiment, a silver layer 50 is provided above the second chalcogenide glass layer 20. A conductive adhesion layer 30 is then provided over the silver layer 50 and a top electrode 22 is provided over the conductive adhesion layer 30. The silver layer 50 may be deposited over the second glass layer 20 by any suitable means, such as sputtering or plating techniques, including electroplating or electroless plating. The desired thickness of the silver layer is about 200 Å. Suitable materials for the conductive adhesion layer include conductive materials capable of providing good adhesion between the silver layer 50 and the top electrode layer 22. Desirable materials for the conductive

adhesion layer 30 include chalcogenide glasses. A top electrode 22 is then formed over the conductive adhesion layer 30.

[0052] The chalcogenide glass layers 17, 20 of this exemplary embodiment can be germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry, where x ranges from 17 to 43. The preferred stoichiometries are about $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$, most preferably about $Ge_{40}Se_{60}$. When the glass is undoped, the first and second chalcogenide glass layers 17, 20 preferably have a thickness from about 100 Å to about 1000 Å and more preferably about 150 Å.

[0053] The metal containing layer 18 can be any suitable metal containing material. For instance, suitable metal containing layers 18 include silver-chalcogenide layers such as silver-selenide, silver-sulfide, silver-oxide, and silver-telluride among others. A desirable metal containing layer is silver-selenide. A variety of processes can be used to form the silver-selenide metal containing layer 18. For instance, physical vapor deposition techniques such as evaporative deposition and sputtering may be used. Other processes such as chemical vapor deposition, co-evaporation or depositing a layer of selenium above a layer of silver to form silver-selenide can also be used. The metal containing layer 18 can be about 1 to 5 times greater than the thickness of the first and second chalcogenide glass layers 17, 20 and is preferably about 470 Å.

[0054] The top and bottom electrodes, 22, 14 can be any conductive material, such as tungsten, tantalum, aluminum, platinum, silver, conductive nitrides, and others. The bottom electrode 14 is preferably tungsten. The top electrode 22 is preferably tungsten or tantalum nitride.

[0055] The conductive adhesion layer 30 may be the same chalcogenide glass material used in the first and second chalcogenide glass layers 17, 20 discussed above. In this case, the conductive adhesion layer 30 can be formed by sputtering the chalcogenide glass onto the silver layer 50. Just as silver is incorporated into a

chalcogenide glass layer when sputter deposited over a silver selenide layer as described above, the energetic nature of the sputtering process may cause a small amount of silver from the silver layer 50 to be incorporated into the chalcogenide glass adhesion layer 30. Thus, the top electrode shorts to the chalcogenide glass adhesion layer 30, creating a conductive path from the top electrode to the first glass layer 17. The desired thickness of a chalcogenide glass conductive adhesion layer 30 is about 100 Å.

[0056] Use of a conductive adhesion layer 30 between the silver layer 50 and the top electrode 22 can prevent peeling of the top electrode 22 material during subsequent processing steps such as photoresist stripping. Electrode 22 materials, including tungsten, tantalum, tantalum-nitride, and titanium, among others, may not adhere well to silver layers 50 such as that shown in FIG. 11. For example, adhesion between the two layers 50, 22 may be insufficient to prevent the electrode 22 layer from at least partially separating (peeling) away from the underlying silver layer 50 and thus loosing electrical contact with the underlying layers 20, 18, 17, 14 of the memory element 100. Poor contact between the top electrode 22 and the underlying memory element layers 20, 18, 17, 14 can lead to electrical performance problems and unreliable switching characteristics. Use of a conductive binding layer 30 can substantially eliminate this problem.

[0057] As discussed above, use of metal containing layers 18, such as silver-selenide, in contact with a chalcogenide glass layer 17 may eliminate the need to dope the chalcogenide glass layer 17 with a metal during formation of the memory element 100. In accordance with the last-discussed embodiment, the silver selenide layer 18 provides a source of silver selenide, which is driven into chalcogenide glass layer 17 by a conditioning step after formation of the memory element 100 (FIG. 11). Specifically, the conditioning step comprises applying a potential across the memory element structure 100 such that silver selenide from the silver selenide layer 18 is driven into the first chalcogenide glass layers 17, forming a

conducting channel. Movement of Ag^+ ions into or out of that channel causes an overall resistance change for the memory element 100. The pulse width and amplitude are critical parameters of the conditioning potential, which generally has a longer pulse width and higher amplitude than a typical potential used to program the memory element. After the conditioning step, the memory element 100 may be programmed, provide that some silver moved into the conductive channel during conditioning.

[0058] When silver is sputtered directly onto silver-selenide, agglomeration of silver at the silver layer 50/silver-selenide layer 18 interface may occur during deposition. Such silver agglomeration can cause subsequent processing problems during operation of the memory cell 100. Use of a chalcogenide glass layer 20 between the silver layer 50 and the silver-selenide layer 18 can prevent silver agglomeration on the surface of the silver-selenide layer 18.

[0059] In another exemplary embodiment of the present invention, an additional silver layer 40 can be deposited between the lower chalcogenide glass layer 17 and the silver selenide glass layer 18, as shown in FIG. 12. Thus, a memory element 200, as illustrated in FIG. 12, comprises a first chalcogenide glass layer 17, a first silver layer 40, a silver-selenide glass layer 18, a second chalcogenide glass layer 20, a second silver layer 50', a conductive adhesion layer 30, and a top electrode layer 22. Addition of the first silver layer 40 minimizes the amplitude and pulse width of the conditioning potential needed prior to write and erase operations. Layers 17, 18, 20, 22, 50', and 30 can be of the same or similar materials as in other embodiments of the invention and can be formed by similar means. Furthermore, the first chalcogenide glass layer 17 may be a doped chalcogenide glass. For example, the first chalcogenide glass layer may be silver-doped silver selenide.

[0060] In accordance with this embodiment of the invention, a conditioning step allows silver selenide from the silver selenide layer 18 to be incorporated into the first chalcogenide glass layer 17. Deposition of the silver

selenide layer 18 over the silver layer 40 causes the silver selenide layer 18 to become silver-rich. This silver-rich silver selenide more easily incorporates into the first chalcogenide glass layer 17 under the influence of an applied conditioning pulse. As a result, the conditioning pulse can have a shorter pulse width and lower amplitude, effectively speeding up the conditioning process.

[0061] The first silver layer 40 must be relatively thin in comparison to the second silver layer 50', in order to prevent an excess of silver from being incorporated into the lower chalcogenide layer during conditioning, which can shorten the life of the memory element. The first silver layer 40 has a desired thickness of about 35-50 Å when the first glass layer 17 is about 150 Å

[0062] As shown in FIG. 13, in accordance with another embodiment of the present invention and similar to the first exemplary embodiment, a silver layer 40' is provided above a chalcogenide glass layer 17. Thus, a memory element 300, as illustrated in FIG. 13, comprises a first chalcogenide glass layer 17, a silver layer 40', a silver-selenide glass layer 18, a second chalcogenide glass layer 20, and a top electrode layer 22. In accordance with this embodiment of the invention, a conditioning step drives silver selenide from the silver selenide layer 18 into the first chalcogenide glass layer 17, opening a conductive channel.

[0063] As shown in FIG. 14, in accordance with another embodiment of the present invention and similar to the embodiment shown in FIG. 13, a silver layer 50' is provided above the second glass layer 20. The silver layer 50' may be deposited over the second glass layer 20 by any suitable means, such as sputtering or plating techniques, including electroplating or electroless plating. The desired thickness of the silver layer is about 200 Å. A top electrode 22 is then formed over the silver layer 50'. Thus, a memory element 400, as illustrated in FIG. 14, comprises a first chalcogenide glass layer 17, a silver layer 40'', a silver-selenide glass layer 18, a second chalcogenide glass layer 20, a second silver layer 50'and a top electrode layer 22. The first chalcogenide glass layer 17, may be a doped

chalcogenide glass. For example, the first chalcogenide glass layer may be silver-doped silver selenide.

[0064] The embodiments described above refer to the formation of only a few possible resistance variable memory element 100 structures in accordance with the invention. It must be understood, however, that the invention contemplates the formation of other such resistance variable memory elements, which can be fabricated as a memory array and operated with memory element access circuits.

[0065] FIG. 15 illustrates a typical processor system 400 which includes a memory circuit 448, for example a programmable conductor RAM, which employs resistance variable memory elements fabricated in accordance with the invention. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory 448 communicates with the system over bus 452 typically through a memory controller.

[0066] In the case of a computer system, the processor system may include peripheral devices such as a floppy disk drive 454 and a compact disc (CD) ROM drive 456, which also communicate with CPU 444 over the bus 452. Memory 448 is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements 100. If desired, the memory 448 may be combined with the processor, for example CPU 444, in a single integrated circuit.

[0067] The above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

Claims:

1. A resistance variable memory element comprising:

a first electrode;

a first chalcogenide glass layer electrically coupled to said first electrode;

a first metal layer over said first chalcogenide glass layer;

a metal containing layer over said metal layer;

a second chalcogenide glass layer over said metal containing layer;

a second metal layer over and in contact with said second chalcogenide glass layer;

a conductive adhesion layer over and in contact with said second metal layer; and

a second electrode electrically coupled to said conductive adhesion layer.

2. The resistance variable memory element of claim 1, wherein said metal containing layer is a silver-chalcogenide layer.

3. The resistance variable memory element of claim 2, wherein said metal containing layer is silver-selenide.

4. The resistance variable memory element of claim 1, wherein said metal containing layer has a thickness of about 1 to 5 times the thickness of the first and second chalcogenide glass layers.

5. The resistance variable memory element of claim 1, wherein said metal containing layer has a thickness of about 470 Å.

6. The resistance variable memory element of claim 1, wherein said first metal layer and said second metal layer are silver.

7. The resistance variable memory element of claim 6, wherein said first silver layer has a thickness of about 35 Å to about 50 Å.

8. The resistance variable memory element of claim 6, wherein said second silver layer has a thickness of about 200 Å.

9. The resistance variable memory element of claim 6, wherein said first chalcogenide glass layer and said second chalcogenide glass layer each have a thickness of about 100 Å to about 1000 Å.

10. The resistance variable memory element of claim 1, wherein said first chalcogenide glass layer comprises silver-doped chalcogenide glass.

11. The resistance variable memory element of claim 1, wherein said first chalcogenide glass layer and said second chalcogenide glass layer each have a thickness of about 150 Å.

12. The resistance variable memory element of claim 1, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise a material having a formula Ge_xSe_{100-x}, where x = 17 to 43.

13. The resistance variable memory element of claim 1, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise germanium selenide glass having a stoichiometry of about $Ge_{40}Se_{60}$.

14. The resistance variable memory element of claim 1, wherein said conductive adhesion layer is a chalcogenide glass layer.

15. The resistance variable memory element of claim 14, wherein said conductive adhesion layer is germanium selenide glass having a stoichiometry of about $Ge_{40}Se_{60}$.

16. The resistance variable memory element of claim 14, wherein said conductive adhesion layer has a thickness of about 100 Å.

17. The resistance variable memory element of claim 1, wherein said first and second electrodes are selected from the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

18. The resistance variable memory element of claim 17, wherein said first electrode is tungsten.

19. The resistance variable memory element of claim 17, wherein said second electrode is tantalum nitride

20. A method of forming a resistance variable memory element comprising:

forming a first electrode;

forming a first chalcogenide glass layer;

forming a first metal layer electrically coupled to said first chalcogenide glass layer;

forming a metal containing layer over said metal layer;

forming a second chalcogenide glass layer over said metal containing layer;

forming a second metal layer over and in contact with said second chalcogenide glass layer;

forming a conductive adhesion layer over and in contact with said second metal layer; and

forming a second electrode electrically coupled to said conductive adhesion layer.

21. The method of claim 20, wherein said metal containing layer is a silver-chalcogenide layer.

22. The method of claim 21, wherein said metal containing layer is silver-selenide.

23. The method of claim 20, wherein said metal containing layer has a thickness of about 1 to 5 times the thickness of the first and second chalcogenide glass layers.

24. The method of claim 20, wherein said metal containing layer has a thickness of about 470 Å.

25. The method of claim 20, wherein said first and second metal layers are silver.

26. The method of claim 25, wherein said first silver layer has a thickness of about 35 Å to about 50 Å.

27. The method of claim 25, wherein said second silver layer has a thickness of about 200 Å.

28. The method of claim 20, wherein said first chalcogenide glass layer and said second chalcogenide glass layer each have a thickness of about 100 Å to about 1000 Å.

29. The method of claim 28, wherein said first chalcogenide glass layer and said second chalcogenide glass layer each have a thickness of about 150 Å.

30. The method of claim 20, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise a material having a formula Ge_xSe_{100-x}, where x = 17 to 43.

31. The method of claim 20, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise germanium selenide glass having a stoichiometry of about $Ge_{40}Se_{60}$.

32. The method of claim 20, wherein said conductive adhesion layer is a chalcogenide glass layer.

33. The resistance variable memory element of claim 32, wherein said conductive adhesion layer is germanium selenide glass having a stoichiometry of about $Ge_{40}Se_{60}$.

34. The method of claim 33, wherein said conductive adhesion layer has a thickness of about 100 Å.

35. The method of claim 33, further comprising the step of applying a conditioning potential across the memory element structure.

36. The method of claim 34, wherein the pulse width of said conditioning potential ranges from about 100 nanoseconds to about 500 nanoseconds.

37. A resistance variable memory element comprising:

a first electrode;

a first chalcogenide glass layer electrically coupled to said first electrode;

a second chalcogenide glass layer over said first chalcogenide glass layer;

a metal containing layer between said first and second chalcogenide glass layers, said metal containing layer having a different composition than said first and second chalcogenide glass layers;

a first metal layer between said first chalcogenide glass layer and said metal containing layer;

a second metal layer over and in contact with said second chalcogenide glass layer;

a third chalcogenide glass layer over and in contact with said second metal layer; and

a second electrode electrically coupled to said third chalcogenide glass layer.

38. The resistance variable memory element of claim 37, wherein said metal containing layer is a silver-chalcogenide layer.

39. The resistance variable memory element of claim 38, wherein said metal containing layer is silver-selenide.

40. The resistance variable memory element of claim 37, wherein said metal containing layer has a thickness of about 1 to 5 times the thickness of the first and second chalcogenide glass layers.

41. The resistance variable memory element of claim 37, wherein said metal containing layer has a thickness of about 470 Å.

42. The resistance variable memory element of claim 37, wherein at least one of said first and second metal layers is silver.

43. The resistance variable memory element of claim 37, wherein said first chalcogenide glass layer and said second chalcogenide glass layer each have a thickness of about 100 Å to about 1000 Å.

44. The resistance variable memory element of claim 37, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise a material having a formula Ge_xSe_{100-x}, where x = 17 to 43.

45. The resistance variable memory element of claim 37, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise germanium selenide glass having a stoichiometry of about $Ge_{40}Se_{60}$.

46. The resistance variable memory element of claim 37, wherein said first and second electrodes are selected from the group consisting of tungsten, nickel, tantalum, aluminum, platinum, silver, and conductive nitrides.

47. The resistance variable memory element of claim 37, wherein said first chalcogenide glass layer comprises silver-doped chalcogenide glass.

48. A method of forming a resistance variable memory element comprising the steps of:

forming a first electrode;

forming a first chalcogenide glass layer electrically coupled to said first electrode;

forming a second chalcogenide glass layer over said first chalcogenide glass layer;

forming a metal containing layer between said first and second chalcogenide glass layers;

forming a first metal layer between said first chalcogenide glass layer and said metal containing layer ;

forming a second metal layer over and in contact with said second chalcogenide glass layer;

forming a third chalcogenide glass layer over and in contact with said second metal layer; and

forming a top electrode electrically coupled to said third chalcogenide glass layer.

49. The method of claim 48, wherein said metal containing layer is a silver-chalcogenide layer.

50. The method of claim 48, wherein said metal containing layer is silver-selenide.

51. The method of claim 48, wherein said metal containing layer has a thickness of about 1 to 5 times the thickness of the first and second chalcogenide glass layers.

52. The method of claim 48, wherein said metal containing layer has a thickness of about 470 Å.

53. The method of claim 48, wherein at least one of said first and second metal layers is silver.

54. The method of claim 48, wherein said first chalcogenide glass layer and said second chalcogenide glass layer each have a thickness of about 100 Å to about 1000 Å.

55. The method of claim 48, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise a material having a formula Ge_xSe_{100-x}, where x = 17 to 43.

56. The method of claim 55, wherein said first chalcogenide glass layer and said second chalcogenide glass layer comprise germanium selenide glass having a stoichiometry of about $Ge_{40}Se_{60}$.

57. The method of claim 48, further comprising the step of applying a conditioning potential across the memory element structure.

58. The method of claim 57, wherein the pulse width of said conditioning potential ranges from about 100 nanoseconds to about 500 nanoseconds.