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ABSTRACT

A method to integrate low dielectric constant dielectric materials with copper metallization is described. A metal line is provided overlying a semiconductor substrate and having a nitride capping layer thereover. A polysilicon layer is deposited over the nitride layer and patterned to form dummy vias. A dielectric liner layer is conformally deposited overlying the nitride layer and dummy vias. A dielectric layer having a low dielectric constant is spun-on overlying the liner layer and covering the dummy vias. The dielectric layer is polished down whereby the dummy vias are exposed. Thereafter, the dielectric layer is cured whereby a cross-linked surface layer is formed. The dummy vias are removed thereby exposing a portion of the nitride layer within the via openings. The exposed nitride layer is removed. The via openings are filled with a copper layer which is planarized to complete copper metallization in the fabrication of an integrated circuit device.

FIGURE 12



