

OBJECT DETECTOR

This invention relates to an object detector. Embodiments of the invention may for example be adapted particularly but not exclusively to provide a means for detecting the positions of studs or other supporting structures within walls.

5 United States patent specification 4,099,118 describes an object detector comprising an electronic switching device the output of which is in use cyclically switchable between at least two different
10 states, said switching device having a capacitance which is in use of the detector cyclically charged and discharged under conditions whereby the rate of charge and/or discharge of the capacitance determines the
15 time interval, for each cycle of the output of said device, for which said output is in one of said states, the rate of charge and/or discharge of said capacitance being influenced, in the presence of an object in the vicinity of the object detector whereby to effect variation of the length of said time
20 interval.

 In the United States patent the capacitance is defined at least in part by a flat plate and direct variation of that capacitance, occurring in the presence of said object is utilized to effect
25 variation of the length of the time interval. The

need to form the capacitance as including a plate imposes manufacturing constraints which may not be desired. For example it is not always convenient to form the detector with a flat plate of substantial area.

An object of the invention is to provide an object detector which permits more flexibility in the manner of formation of the capacitance.

Thus, the invention in one form is characterised by the provision of first means in use providing an electric field therearound, said first means being arranged whereby in use of the detector said electric field is at least partially discharged in the presence of a said object in the vicinity of said first means to effect said influencing of the rate of change and/or discharge of said capacitance. By this construction it is not necessary to form the capacitance as a plate. In one particularly preferred form of the invention, the switching device is formed as a free running multivibrator, the output of which comprises said output of the switching device and which output is switched alternately between two states, such as on and off states, and wherein the rate of charge or discharge of the said capacitance effects said variation is the length of said time interval by determining the length of time for which the output is in at least a particular said state during each cycle, such as by determining the length of the on and/or off parts of each cycle of output of the multivibrator. Such a free running multivibrator may include a Schmitt gate device, the output of which comprises said output of the switching device, said Schmitt gate device being of a kind in which the output is conditioned to a first state when the input

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thereof is at one state and whereupon on traverse of the state of the input from said one state to another state the output is switched to a second state on said input reaching said second state, said output being
5 connected to said input via a feed-back network coupled whereby in use to revert said input to said one state when said output is conditioned to said second state. Usually, the Schmitt gate device is a Schmitt inverter gate in which case said one state and
10 said second state are low states and said another state and said first state are high states. Said capacitance may provide a connection between said input and one side of an electric supply for said detector and an impedance may be provided between the
15 other side of said supply and said input. In this case, the placing of said input in said one state may act to discharge said capacitance and said capacitance may be caused to remain in its uncharged state until the output is next placed in said first state pursuant
20 to operation of the Schmitt gate device, whereafter said capacitance is charged through said impedance from said supply to cause said input to be conditioned progressively towards said another state until said another state is reached, whereafter the output is
25 again conditioned to said second state for initiation of another cycle of operation, whereby the parts of each cycle of the output device for which the output of said Schmitt gate device is in its second state are dependent on the rate of charge of said capacitance.
30 In this case, the said first means is coupled to the input of said Schmitt gate device and operates to effect partial diversion of charging of said capacitance to an extent dependent on whether or not

an object is present in the vicinity thereof. The first means may comprise an electrode.

The feedback network may for example include a diode arranged to permit conduction from said input to said output in parallel to said Schmitt gate device under the condition that the input is in said another state and the output is in said second state, but to preclude such conduction when the output is in said first state. A resistance or other impedance may be provided in series with said diode.

In a preferred form of the invention, a reference device which may be otherwise similar to the detector above described is provided arranged whereby in use to provide an output which can at least be adjusted so as in the absence of an object in the vicinity of said first means to be substantially in phase with said output of said free running multivibrator but arranged whereby introduction of the object to the vicinity of said first means differentially effects the free running multivibrator and said reference device whereby, for the free running multivibrator, the length of the said time interval during at least one cycle of the output thereof is varied as compared to the length of the corresponding time interval for the output of the reference device, whereby the presence of said object can be detected by detecting the condition where the outputs of the free running multivibrator and reference device are not momentarily in the same state. In this case, the free running multivibrator and reference device are preferably interconnected so as to synchronise the time of beginning of each cycle of the outputs thereof. In another embodiment, the reference device is provided with second means similar to said first means for

varying a said time interval for the output thereof, corresponding to the said time interval, the length of which is varied by influencing the rate of change and/or discharge of said capacitance.

5 The invention may also be implemented using a comparator arranged to switch the output state thereof when the signal on one input thereof exceeds a reference level applied to the other input, said one input being connected to said capacitance, said
10 capacitance being arranged to permit progressive charging thereof when the output of the comparator is in one state during each cycle thereof, and to effect discharging thereof when the output of the comparator is subsequently in another state during each cycle of
15 operation thereof, whereby the time period between said one input of the comparator reaching said reference level and the effecting of discharge of said capacitance is dependent on the rate of charging of said capacitance, said time interval being the time on
20 each said cycle for which said output of said comparator is in said one or said another state. That is to say, in this case, the output of the comparator changes state for a said interval on each cycle of the comparator output. The first means may in this case
25 be connected to said one input to effect variation of said time interval when an object is near thereto. Embodiments of this kind may be provided with a reference comparator otherwise operating in a similar way to the first mentioned comparator.

30 The invention is further described with reference to the accompanying drawings in which:

Figure 1 is a circuit diagram of an object detector constructed in accordance with the invention;

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Figure 2 is a timing diagram showing wave forms in use generated in the detector of figure 1;

Figure 3 is a circuit diagram of an alternative form of detector constructed in accordance with the invention;

Figures 4 and 5 are timing diagrams illustrating wave forms appearing in the circuit of figure 3 under two different conditions of operation thereof;

Figure 6 is a circuit diagram of a further detector constructed in accordance with the invention; and

Figure 7 is a timing diagram showing wave forms appearing in the circuit of figure 6 under one operating condition thereof;

Figures 8 and 9 are circuit diagrams of two further alternative forms of detector constructed in accordance with the invention; and

Figure 10 is a diagram showing a possible form of electrodes for incorporation into the detector of figure 6.

The object detector 10 for which the circuit is shown in figure 1 includes a Schmitt inverter gate G1 having its input connected via a resistor R1 to a positive supply line 12. The output of the gate G1 is connected to the input via a feedback network comprising a resistor R2 and a diode D1 connected in series. The diode D1 has its anode connected to the input of gate G1. A sensing electrode 14 is connected to the input to the gate G1.

The Schmitt inverter gate G1 is characterised in that when the input signal thereto exceeds a predetermined level, the output level changes from a pre-existing high level to a low level. Similarly, when the input signal magnitude drops below the

predetermined level the output rises to a high level. The output signal waveform is otherwise independent of the input signal waveform.

The detector 10 is dependent for its operation on the existence of stray capacitance between terminals of the gate G1. Although the interaction of these stray capacitances with other integers of the circuit may be complex, the mode of operation of the circuit of the detector 10 can be understood by considering only the stray capacitance C1 as existing between the input to the gate G1 and the negative supply line 16. Assuming firstly that the capacitor C1 is discharged and that the voltage conditions of the diode D1 are such as to preclude conduction thereof, the capacitor C1 will charge via the resistor R1 so that the voltage on the input to the gate G1 will rise from a low value progressively with time to a high value. This rise is shown by reference numeral 17 in the waveform of the gate input signal V_{in} to the gate as depicted at "a" in figure 2. During this time, the output from the gate G1 is in at a high condition as indicated at 23 in the waveform of the gate output signal V_{out} shown at "b" in figure 2. After a time interval t_1 the voltage on the input to gate G1 rises to a threshold level indicated by the phantom line 19. After a further time interval therefrom, denoted by t_2 , the output condition of the gate G1 is altered to a low state as indicated by reference numeral 21 at "b" in figure 2. Whilst, previously, the diode D1 was rendered non-conductive because the output from the gate G1 was at a high state the fall in the gate output to its low state has the effect that the diode has its anode, at the input to the gate G1, at a higher potential than the cathode, so that the diode

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becomes conductive whereby the capacitor C1 is discharged quickly through the diode D1 and resistor R2 to the output of the gate G1. Thereafter, after a time interval t_3 from discharge, the output of the gate G1 is again placed in a high state and a new cycle of operation begins with a fresh charging of the capacitor C1. The time interval t_2 after reaching the threshold 19 and before discharge of capacitor C1 begins is due to internal delays within the gate G1 which cause the switching of the output to occur at a later time than the alteration of the input state which causes that output switching. Similarly, the time interval t_3 after the output reaches the low state and before the high state is regained after discharge of the capacitor C1 is due to internal delays in the gate which hold the output in the low state for a short time notwithstanding that the input state is low pursuant to discharge of the capacitor C1. Correspondingly the input to the gate G1 is held low for the time period t_3 as shown at 25 in the input signal waveform.

The device 10 thus comprises in essence a free running astable multi-vibrator, the input and output waveforms of which comprise repetitive cycles as are represented at 27 and 29 respectively in the waveforms at "a" and "b" in figure 2. During each cycle of the output signal, the gate output exhibits a negative going pulse 29a of interval approximately equal to t_3 .

The electrode 14 is arranged in any convenient form such as in the form of a conductive wire or plate arranged to generate an electric field therearound pursuant to application of signal thereto during charging of the capacitor C1 in each cycle of the input signal, so that when an object such as a

non-conducting object is brought into proximity to the electrode the charge on the electrode tends to be dissipated. By this means, the rate of charge of the capacitor C1 during the charging period of each cycle is relatively decreased so that the time interval t_1 is increased as compared with the static condition where no object is nearby. The extent to which this effect occurs is dependent upon various factors such as the overall impedance levels prevailing in the circuit, particularly the values of R1 and C1 and the repetition rate of the oscillator represented by the gate circuit. Generally, frequencies of the order of 2 MHz may be employed. Resistance R1 may be chosen to be of large value, such as 2 M Ω with commercially available devices G1 such as type 74C14.

Figure 3 shows a detector 31, being a modification of the arrangement of figure 1. Here there are two Schmitt inverter gates A1 and A2. Gate A1 has its input connected via a resistor R3 to a positive supply line 22 whilst gate A2 has its input connected via a resistor R4 to the moving contact of a potentiometer VR5, the latter being connected between two further resistors R6, R7 in a series network across the positive supply line 22 and negative supply line 24. The inputs of the two gates A1 and A2 are connected to the outputs via respective feedback loops which include a common resistor R8. More particularly, the feedback loop for gate A1 includes a diode D2 having its anode connected to the input to the gate A1 and its cathode connected to one end of resistor R3. The other end of resistor R8 is connected to the output of gate A1 via a further diode D3. The feedback loop for gate A2 includes a diode D4 having its anode connected to the gate input. The cathode of the diode D4 is

connected to the same end of resistor R8 as diode D2. The other end of resistor R8 is connected to the output of gate A2 via a diode D5. Diodes D3, D5 have their anodes connected to resistor R8 and their cathodes connected to the outputs of the respective gates A1, A2. The outputs of the two gates A1 and A2 are also connected via respective resistors R9, R10 to the collector and base respectively of a transistor TR1, the emitter of the transistor TR1 being connected to the negative supply line 24. Output from the circuit is taken via an output line 28 connected to the collector of transistor TR1. Transistor TR1 is NPN type such as type 2N3904. An electrode 30 similar to the electrode 14 previously described is connected to the input to gate A1.

In normal operation of the detector 31, the two gates A1 and A2 function in the same way as the previously described gate G1. The capacitances between the inputs of the gates A1 and A2 and negative supply line 24, represented as C2 and C3 respectively, being repeatedly charged and discharged to produce input pulse waveforms for the gates A1, A2 respectively as indicated at (a) and (c) in figure 4 whilst the output signals have corresponding waveforms as indicated at (b) and (d) respectively in figure 2. In figure 4, reference numerals corresponding to those used in figure 2 have similar meanings to those ascribed thereto in the description of figure 2.

If the gates A1 and A2 are electrically similar and the remaining components of the respective parts of the circuits associated with the gates A1 and A2 are similar the rates of increase of the input voltages at the portions 17 of each cycle thereof will be the same for each gate in the case where electrode

30- is not near an object, or can be made the same by adjustment of potentiometer VR5. The threshold voltages will also be similar so that the input waveforms for both, as indicated at "a" and "c" in figure 4, will be the same and of the same duration, whilst the output waveforms will likewise be of the same with similar durations of the respective on and off intervals as shown at "b" and "d" in figure 4. Discharge of the capacitances C2, C3 associated with the respective gates A1, A2 occurs in this instance through respective diodes D2 and D4, as well as through the common resistor R8 and a respective one of the diodes D3 and D5 when the respective gate outputs are in low conditions. Because of this arrangement, the result is achieved that in the event that the input of one of the gates A1 and A2 should for some reason reach its threshold voltage before the other, a discharge path will be provided for the capacitances C2 and C3 associated with both of the two gates. For example in the case where the gate A1 has its output placed in a low state, a discharge path will be provided for capacitance C2 via diode D2, resistor R8 and diode D3. Similarly, the gate A2 will then have its capacitance C3 discharged through diode D4, resistor R8 as well as diode D3. In the converse case where gate A2 first has its output placed in a low state, diode D5 provides a discharge path for the capacitances C2, C3 of both gates.

Figure 5 shows input and output voltages for the two gates A1 and A2 for the condition where gate A1 reaches its threshold voltage before gate A2. The input signals for the gates A1 and A2 are shown respectively at "a" and "c" in figure 5, whilst the output voltages are shown respectively at "b" and "d"

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in figure 5. In figure 5, reference numerals like those used in figure 2 denote similar features.

In this instance, because of a supposed greater charging rate of the capacitance C2 associated with gate A1, the part 17 of the waveform of the input voltage V_{in} to gate A1 is relatively of greater slope than that of the corresponding part 17 of the input voltage V_{in} to the gate A2. Thus, the time interval t'_1 , being the interval between initiation of charging of capacitor C2, and the reaching of the threshold voltage denoted by line 19 is relatively less than the corresponding interval t_1 for the other gate. Following the interval t'_1 , the output of the gate A1 is reverted to its low state after the time interval t_2 as previously described and then, after an interval equal to the previously described interval t_3 , the output of gate A1 is again reverted to its high state. However, the capacitance C2 does not begin immediately charging after such reversion to the high state of the output of gate A1 because that input is maintained in a low state for a further time interval for the reason now described. More particularly, referring to the output voltage waveform of gate A2 at "d" in figure 5, it will be seen that because the threshold voltage for the gate A2 is not reached until the time interval t_1 which is greater than the time interval t'_1 the output of gate A2 is not conditioned to its low state until a somewhat later time than the corresponding conditioning of the output of gate A1 to the low condition. It should be borne in mind that the placing of the output of gate A2 is a low condition will occur after the same interval as before, namely interval t_2 , from the passing of the threshold voltage on the input. This interval is as mentioned fixed by the internal

configuration of the gates. Thus even though the capacitance C3 will immediately be discharged when gate A1 has its output conditioned to the low state, that is say simultaneously with the discharge of capacitance C3 associated with gate A1, recharging of both the capacitances C2 and C3, cannot begin until after a time interval t_3 from the time of expiration of the combined intervals $(t_1 + t_2)$. Interval t_3 is, again, as previously mentioned, a fixed time interval. Only when the time interval t_3 has passed for the gate A2 will the output of gate A2 be reverted to its high state whereupon the capacitances C2 and C3 are left with no discharge route through either diode D3 and charging of both capacitances C2 and C3 will begin at the same time. The period for which the input voltage to gate A1 is held low is correspondingly lengthened as compared with that prevailing for gate A2.

A result of the above is that in the condition mentioned, where gate A1 reaches its threshold before gate A2, the intervals for which the outputs of the gates A1 and A2 are held negative, whilst being of the same duration (about equal to interval t_2) no longer coincide exactly as in the case where outputs of the two gates are simultaneously conditioned at high or low states.

The transistor TR1 operates to detect a condition where there is phase alteration between the parts of each cycle of the outputs of the two gates for which the outputs are negative. More particularly, the transistor TR1 is operable to provide a high output only under the condition where the output from gate A1 is high and output from gate A2 is low. In other conditions of outputs from A1 and A2, the output from transistor TR1 is low. Thus, during normal operation,

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the outputs A1 and A2 will be in phase so that the collector and base voltages of transistor VR1 will always be the same as each other and no output will result from transistor TR1. When there is a phase displacement between the output signals, there will still be a substantial period of time during each cycle of operation of the device where the outputs likewise are the same, either high or low. However in the case indicated where the output of gate A1 is advanced in phase relative to gate A2 there will be short time interval corresponding to the beginning of each negative going part 29a of the cycle of output from gate A1 where the output of gate A1 is low and the output of gate A2 is high and a later period, at the end of the corresponding negative part 29a of the cycle of the output of gate A2 where the output of gate A2 is low and the output of gate A1 is high. The former of these two situations will not give rise to an output from transistor TR1, but the latter will result in generation of a short output pulse from the transistor TR1. Thus, where there is a consistent phase difference between the outputs of the gates A1 and A2 there will be a train of pulses generated at the output of transistor TR1, these occurring at times corresponding to the end part of each negative going part 29a of the cycle of the output from gate A2. Similarly, in the event that gate A2 should reach its threshold before gate A1, there will be a pulse from the output of transistor TR1 this occurring at the trailing portion of each negative going cycle part of the output of gate A1.

It will be noted from figure 4 that the electrode 30 is connected to the input of gate A1 and thus, by the mechanism previously described, the charging rate

of the capacitance C2 associated with gate A1 will be altered in accordance with whether or not discharge of the electric charge on the electrode 30 occurs so in turn being influenced by whether or not an object is in the vicinity of the electrode 30.

To use the device shown in figure 4, the potentiometer VR5 is first adjusted, when no object is in the vicinity of electrode 30, so that the output and input voltages of the two gates A1 and A2 are as represented in figure 3, that is to say so that the outputs are in phase whereby no output is derived from transistor TR1. Then, when an object is moved into into the vicinity of the electrode 30 the charging rate of the capacitance C2 associated with gate A1 is slowed so that gate A1 reaches its input threshold on each cycle of operation at a later stage than gate A2 so giving rise to an output pulse train from transistor TR1. The pulse train from the output of transistor TR1 may be passed to a suitable detecting circuit. In particular, such a circuit may comprise an integrating circuit operable to integrate pulses when present on output line 28 and trigger a suitable relay or other switching device for operating a warning device such as a lamp.

Figure 6 shows the circuit of a further detector 41. In this case, there are again two Schmitt inverter gates A3, A4 similar to the gates A1 and A2 previously mentioned. Gate A1 has its input connected via a resistor R11 to a positive supply line 32 whilst gate A4 has its input connected via a resistor R12 to the movable contact of a variable resistor VR13. Variable resistor VR13 is connected at one end to a resistor VR14 and at the other to a resistor VR15. This series circuit comprised of resistors R14, R15

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and variable resistor VR13 is connected across positive supply line 32 and a negative supply line 34. The inputs of gates A3 and A4 are connected via respective feedback loops, including a common resistor R16, to the outputs thereof. More particularly the input of gate A3 is connected to the anode of a diode D6, the cathode of the diode D6 being connected to one end of a resistor R16. The other end of the resistor R16 is coupled to the cathode of a diode D7, the anode of that diode being connected to the output of the gate A3. The input of gate A4 is connected to the anode of a diode D8, the cathode of that diode being connected to the same end of resistor R16 as diode D6. The output of the gate A4 is connected to the anode of a further diode D9, the cathode of which is connected to the same end of resistor R16 as is diode D7. The junction between diodes D7, D9 and resistor R16 is connected to negative supply 34 via a resistor R17. The outputs from the gates A3 and A4 are connected via respective resistors R18, R19 to the collector and base respectively of a transistor TR2, the emitter of which is connected to the negative supply line 34 and the collector of which is also connected to an output line 42. The stray capacitances from inputs to negative supply are shown at C4, C5 for the respective gates A1, A2.

In this case separate electrodes 44, 46 are coupled to the inputs to the gates A3 and A4 respectively. The resistors R11, R12 and R16 and R17 are selected so that under the condition of the outputs of the gates A3, A4 being high, there is insufficient current flow through diodes D6, D8 and resistors R16, R17 to prevent charging of the stray capacitances C4, C5 associated with the two gates. Thus, under

conditions where no objects are near to either electrode 44 or electrode 46, so that no leakage of charge occurs therefrom, the capacitors C4, C5 may charge to the threshold values of the two gates, at least under a condition of appropriate setting of the potentiometer VR13. Under this circumstance, with the output of the gates A3 and A4 both high, current can flow from positive supply through the gate outputs through the diodes D7 and D9 and through the resistor R17. Thus the interconnection of the diodes D7, D9 and resistor R16 is maintained at a high value. It will be appreciated that this situation will prevail so long as at least one of the outputs of the gate A3 and A4 remains high. For example if the output of the gate A3 should go low, although the anode of the diode D7 will then low, the current flow through resistor R17 will be unaffected since flow can continue from positive supply via the output of gate A4 and diode D9. On the other hand, under the circumstance where both gate outputs are low, there will be no current flow through resistor R17 due to flow from the gate outputs, this flow then being blocked by both diodes D7, D9 which are then reversely biased. Under this circumstance, the junction between resistors R16 and R17 is freed from being tied to a high condition so that diodes D6 and D8 will be forwardly biased permitting current flow through resistor R16 and thence to negative supply line 34 via resistor R17, so discharging capacitors C4, C5. This discharge will continue until a predetermined low state of the gate inputs is reached at which the voltage at the inputs to the two gates A3, A4 will be a proportion of the voltage between positive and negative supply lines 32, 34. By appropriate selection of resistors R11, R12,

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R16 and R17 the voltage to which the capacitors are so discharged may be made arbitrarily low. This may be accomplished, for example, by making the values of R11 and of the equivalent resistive network between positive supply 32 and the input to gate A2 much greater than the sum the values of resistors R16 and R17. Of course, the value of R17 must in this event also be chosen to be sufficiently large as compared with the effective impedance between the positive supply line 32 and the outputs of the gates A3, A4, when these are in the high condition, to permit maintenance of the reverse bias of the diodes D6, D8 in the high condition of output from a gate A3 or A4.

In figure 7 shows, at "a" and "c" input waveforms for gates A3, A4 respectively for the condition where the input of the gate A4 reaches the threshold level of that gate before the input level of the gate A3 reaches the threshold level of gate A3. The reaching of the threshold level for gate A4 is shown as occurring at the time interval t_1 after the beginning of an input waveform cycle. The output of that gate A4 is then placed in a low condition after the following time interval t_2 as before. However, this does not result in immediate discharging of the capacitor C5 because of the aforedescribed holding of the junction between resistors R16 and R17 at a high condition whilst the output of gate A3 remains in a high condition. When later, at the expiration of the time interval t_1 from the beginning of the cycle, the input to the gate A3 reaches its threshold, the output thereof is, after the further time interval t_2 , placed in the low condition as shown. Then, pursuant to both outputs being low, the two capacitances C4 and C5 are immediately discharged simultaneously. After a

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further time interval of t_2 the outputs of gates A3 and A4 revert substantially simultaneously to the high state. Although the total cycle length ($t_1' + t_2 + t_3$) for gate A3 or ($t_1 + t_2 + t_3''$) for gate A4 remains the same for each gate, it will be seen that the interval in each cycle for which the gate A4 remains in the low state is longer than the corresponding interval for the gate A3. Again, then, there is a time for which the output states of the two are not the same, this being a time before beginning of the negative going part of the cycle of the output of gate A3 and after the start of the corresponding part of the cycle of the output of gate A4. During this period, the output of gate A4 is low while that of gate A3 is high. Accordingly, as previously, this constitutes a state at which transistor TR2 is conditioned to the off state as compared with all other states where the output is conditioned to an on state. Thus, for each cycle of operation in which there is a difference in the time intervals t_1'' and t_1 there will be a corresponding pulse on the output of transistor TR2 which may be used, as previously described, to detect a condition where the outputs of the two gates are not exactly in synchronism. The arrangement of figure 6 is particularly advantageous in that it permits the charging rates of the capacitances C4, C5 to be affected by discharge of charge from either electrode 44 or 46. In practice, the electrode 46 may be used to compensate such that the detector remains insensitive to changes in dielectric constant of an object in the vicinity of both electrodes.

Figure 8 shows further detector 61 in accordance with the invention. The detector 61 includes an oscillator

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49 in the form of an operational amplifier 50. A resistor R20 is connected from one input of amplifier 50 to the output thereof, and a second resistor R21 is connected from the other input to the output thereof, the last mentioned input also being connected to negative supply via a capacitor C6. The output from the oscillator 49 is connected via separate diodes D10, D11 to respective inverting inputs of two comparators A5, A6 constituted by operational amplifiers. The inverting input of comparator A5 is connected to positive supply via a resistor R22 and to an electrode 52. The non-inverting input of the comparator is connected via a resistor R23 to positive supply and to negative supply via a resistor R24. The resistors R23, R24 thus constitute a voltage divider operable to tie the non-inverting input to a fixed reference potential. The stray capacitance from the inverting input of comparator A5 to negative supply is shown as a capacitance C7. The non-inverting input of comparator A6 is connected to positive supply via a resistor R25 whilst the inverting input is connected to positive supply via a resistor R26 connected to the movable contact of a potentiometer VR27 itself connected between positive and negative supply. The non-inverting input of comparator A6 is connected to negative supply via a resistor R28. Resistors R25 and R28 constitute a potential divider operable to maintain the non-inverting input of comparator A6 at a reference potential which is fixed and which may be selected to be the same as the potential to which the non-inverting input of comparator A5 is held. The stray capacitance from the inverting input of comparator A6 to negative supply is indicated by reference C8. The outputs of the comparators A5, A6

are connected via respective resistors R29; R30 to the collector and base respectively of a transistor TR3 having its emitter connected to negative supply. The output from the transistor TR2 is taken from the collector via line 54.

In use of the detector 61, the oscillator 49 constituted by operational amplifier 50 and associated components generates a cyclic output during cycles of which the output is for one part maintained low and for a second part maintained at a high condition. When the output from the oscillator is in a high condition no current flow will occur through the diodes D10 and D11 which are reversely biased. During this condition, however, the capacitors C7 and C8 may charge respectively through resistor R22 and through resistor R26 and that part of variable resistor of VR27 between resistor R26 and positive supply. When the voltage on the capacitors C7 and C8 exceeds the reference voltages applied to the non-inverting terminals via the resistive networks connected thereto, the comparators operate to condition the outputs thereof to a low state as opposed to a high state prevailing before such a voltage is reached. Thus, if the capacitors C7 and C8 charge at the same rate from the same initial charge state, and the reference voltages for the comparators are the same, the outputs will be placed simultaneously in a low condition. Subsequent to this, when the output of oscillator 49 is conditioned to a low state, the two capacitors C7 and C8 can discharge through the respective diodes D10 and D11 to negative supply. Thus the voltage on the capacitors C7 drops abruptly whereupon the outputs of the two comparators are reverted to high states. Thereafter, a subsequent cycle of

operation is initiated when the oscillator output again rises to a high state. Thus, in the condition where the rates of charge of the capacitors C7 and C8 are the same and the initial start charges are the same for each cycle, the outputs from the two comparators as directed to the transistor TR3 via the resistors R29 and R30 will be similar and in phase, and will consist of repetitive cycles in which during each cycle the output from each comparator is in a high state except for short negative going pulses occupying a time period after the charge on the respective capacitor C7 or C8 has reached the reference voltage and before discharge of that capacitor by operation of the oscillator 49. In the event, however, that the rate of charge of the capacitor C7 should differ from that of capacitor C8, the voltage on the non-inverting input of one of comparators A5 or A6 will reach the reference level before that of the other so that its output will be conditioned to a high state for a relatively longer period of time before subsequently being reverted to a low state pursuant to discharging of the capacitors C7 and C8, which discharging in any event occurs substantially simultaneously under control of the oscillator. As before, the transistor TR3 is responsive to a condition where the output of comparator A5 is high and that of comparator A6 is low to generate an output on line 54 therefrom. It will be seen that where capacitor C7 charges at a slower rate due to charge loss via electrode 52, there will be a time period between the leading edges of both negative going output pulses in a cycle where the output of comparator A6 will be low and where the output of the comparator A5 will still be high pursuant to that

comparator output not yet being placed in a low state. As in the previously described detectors, then, the presence of an object near electrode 52 will cause charge loss which will result in generation of output pulses on output line 54.

Figure 9 shows a still further detector, wherein an oscillator 58 is constituted by a Schmitt gate G3 having its output connected to its input by a resistor R31 and having its input connected to negative supply via a capacitor C9. The output from the oscillator 58 is connected via diodes D12, D13 to inputs of respective Schmitt inverter gates A7, A8. The input of gate A7 is connected to positive supply via a resistor R32. Gate A8 has its input connected via a resistor R33 to the movable contact of a potentiometer VR34 having one end connected to negative supply and the other end connected to positive supply. The input to gate A7 is connected to an electrode 60. The stray capacitances associated with each gate A7, A8 are shown at C10, C11 respectively. A transistor TR4 has its collector connected via a resistor R35 to the output of gate A7 and its base connected via a resistor R36 to the output of gate A8. Output from the transistor TR4 is taken on an output line 62. The operation of the arrangement of figure 9 is similar to that of figure 8. The oscillator 58 produces repetitive cycles of output, for one part of which the output of the oscillator is high and for another part of which the output is low. If potentiometer VR34 is adjusted so that both gates A7, A8 operate in synchronism, the two capacitances C10, C11 charge via, on the one hand, the resistor R32 and, on the other hand, via the potentiometer VR34 and the resistors R33 until the threshold voltages of the gates A7, A8 are reached

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whereafter the outputs thereof are switched from
formerly prevailing high states to low states. The
timing of the high and low parts of each cycle of
operation of the oscillator are arranged so that after
5 the outputs are so placed in low states the
capacitances C10, C11 are discharged by placing of the
oscillator output in a low state, the discharge
occurring through diodes D12 and D13 whereafter the
output of the gates A7, A8 are again reverted to a
10 high state. In the case where one capacitance C10 or
C11 charges faster than the other, the associated gate
will have its output placed in a low state first and
will thus be caused to remain in that low state for a
longer period until discharge of the capacitances C10
15 and C11 occurs than would be the case for the other
gate. Thus, for each cycle of operation of the
oscillator 58 there will be for each gate A7, A8 a
negative going output pulse, with the pulse of one
gate being longer than the other in the instance where
20 the charging rates of the capacitances C10 and C11
differ. Thus, if the potentiometer VR34 is adjusted
so that with no object in the vicinity of electrode 60
the pulses produced from the gates A7, A8 are of the
same duration, the durations will differ one relative
25 to the other in the case where an object is brought
near the electrode 60 to effect partial discharge of
the charge thereon. As before, the difference in
pulse lengths is effective to condition the output of
the transistor TR4 to provide output pulses only when
30 pulses from gate A7 are longer than of gate A8.

The detectors shown in any one of figures 1, 3, 6, 8
or 9 may be encompassed in a suitable casing together
with a suitable power supply, as well as switch and

alarm circuitry including for example a warning light as previously described. The electrode or electrodes may be positioned adjacent one surface of the casing and the casing adapted to be hand held and moved over surfaces such as over the surface of a wall. The extent to which charge is discharged from the electrodes 14 during such movement will be dependent upon physical parameters associated with the material defining the surface over which the device is moved. Thus, it has been found that the detector is suitable for sensing the presence of wooden studs behind plaster walls and for detecting other objects such as metal objects in walls. The embodiment of figure 6 has been found to be particularly effective in the latter instance since the provision of the two electrodes tends to minimise the detection of dielectric constant variations so that the detector is simply responsive to variations in the form of objects hidden within the wall.

In practice, electrodes 14, 30, 44, 46, 52 and 60 may be formed as wire coils, although other forms may also be used. By way of example figure 10 shows the electrodes 44, 46 of the detector of figure 6 as being so constituted by elongated wire coils L1, L2 respectively. Coil L1 is connected at one end to the input to gate A3 and at the other end to negative supply line 34 via a capacitor C12. Coil L2 is connected at one end to the input of gate A4 and at the other end to negative supply line 34 via capacitor C13. The coils L1, L2 are preferably arranged coaxially with coil L1 being within coil L2. For example, L1 may be formed of about 50 turns of wire of thickness sufficient to maintain rigidity so as to form a helix of about 2cm diameter. Coil 46 may for example be formed

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of similar wire, defining a helix of about 3cm diameter and comprised of about ten turns. •

5 Whilst in the described arrangements, the transistors TR1, TR2, TR3 and TR4 are NPN types, these transistors could alternatively be replaced by suitable PNP types such as type 2N3906.

The described arrangements have been advanced merely by way of explanation and many modifications may be made thereto.

CLAIMS

1. An object detector comprising an electronic switching device the output of which is in use
5 cyclically switchable between at least two different states, said switching device having a capacitance which is in use of the detector cyclically charged and discharged under conditions whereby the rate of charge and/or discharge of the capacitance determines the
10 time interval, for each cycle of the output of said device, for which said output is in one of said states, the rate of charge and/or discharge of said capacitance being influenced, in the presence of an object in the vicinity of the object detector whereby
15 to effect variation of the length of said time interval, the detector further including first means in use providing an electric field therearound, said first means being arranged whereby in use of the detector said electric field is at least partially
20 discharged in the presence of a said object in the vicinity of said first means to effect said influencing of the rate of charge and/or discharge of said capacitance.
- 25 2. An object detector as claimed in claim 1 wherein the switching device is formed as a free running multivibrator, the output of which comprises said
30 output of the switching device and which output is switched alternately between two states and wherein the rate of charge or discharge of the said capacitance effects said variation is the length of said time interval by determining the length of time for which the output is in at least a particular said state during each cycle.



3. An object detector as claimed in claim 2 wherein said free running multivibrator includes a Schmitt gate device, the output of which comprises the output of the switching device, said Schmitt gate device being of a kind in which the output is conditioned to a first state when the input thereof is at one state and whereupon on traverse of the state of the input from said one state to another state the output is switched to a second state on said input reaching said second state, said output being connected to said input via a feed-back network coupled whereby in use to revert said input to said one state when said output is conditioned to said second state.

4. An object detector as claimed in claim 3 wherein said Schmitt gate device is a Schmitt inverter gate and said one state and said second state are low states and said another state and said first state are high states.

5. An object detector as claimed in claim 4 wherein said capacitance provides a connection between said input and one side of an electric supply for said detector and an impedance is provided between the other side of said supply and said input.

6. An object detector as claimed in claim 5 arranged whereby the placing of said input in said one state acts to discharge said capacitance and said capacitance is caused to remain in its uncharged state until the output is next placed in said first state pursuant to operation of the Schmitt gate device, whereafter said capacitance is charged through said impedance from said supply to cause said input to be



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conditioned progressively towards said another state until said another state is reached, whereafter the output is again conditioned to said second state for initiation of another cycle of operation, whereby the parts of each cycle of the output device for which the output of said Schmitt gate device is in its second state are dependent on the rate of charge of said capacitance.

7. An object detector as claimed in claim 6 wherein the said second means is coupled to the input of said Schmitt gate device and operates to effect partial diversion of charging of said capacitance to an extent dependent on whether or not an object is present in the vicinity thereof.

8. An object detector as claimed in any one of claims 5 to 7 wherein said feedback network includes a diode arranged to permit conduction from said input to said output in parallel to said Schmitt gate device under the condition that the input is in said another state and the output is in said second state, but to preclude such conduction when the output is in said first state.

9. An object detector as claimed in claim 8 wherein an impedance is provided, in said feedback loop, in series with said diode.

10. An object detector as claimed in any one of claims 2 to 9 including a reference device arranged whereby in use to provide an output which can at least be adjusted so as in the absence of an object in the vicinity of said first means to be substantially in



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phase with said output of said free running multi-vibrator but arranged whereby introduction of the object to the vicinity of said first means differentially effects the free running multivibrator and said reference device whereby, for the free running multivibrator, the length of the said time interval during at least one cycle of the output thereof is varied as compared to the length of the corresponding time interval for the output of the reference device, whereby the presence of said object can be detected by detecting the condition where the outputs of the free running multivibrator and reference device are not momentarily in the same state.

11. An object detector as claimed in claim 10 wherein the free running multivibrator and reference device are interconnected so as to synchronise the time of beginning of each cycle of the outputs thereof.

12. An object detector as claimed in claim 10 or 11 wherein the reference device is provided with second means for varying a said time interval for the output thereof, corresponding to the said time interval, the length of which is varied by influencing the rate of change and/or discharge of said capacitance.

13. An object detector as claimed in claim 1 including a comparator arranged to switch the output state thereof when the signal on one input thereof exceeds a reference level applied to the other input, said one input being connected to said capacitance, said capacitance being arranged to permit progressive charging thereof when the output of the comparator is in one state during each cycle thereof, and to effect



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discharging thereof when the output of the comparator is subsequently in another state during each cycle of operation thereof, whereby the time period between said one input of the comparator reaching said
5 reference level and the effecting of discharge of said capacitance is dependent on the rate of charging of said capacitance, said time interval being the time in each said cycle for which said output of said comparator is in said one or said another state.

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14. An object detector as claimed in claim 13 wherein the first means is connected to said one input to effect variation of said time interval when an object is near thereto.

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15. An object detector as claimed in claim 14, including a reference comparator arranged in use to provide an output which can at least be adjusted so as in the absence of an object in the vicinity of said
20 first means to be substantially in phase with said output of said the first mentioned comparator, but arranged whereby introduction of the object to the vicinity of said first means differentially effects the comparators, whereby for the first mentioned
25 comparator, the length of the said time interval during at least one cycle of the output thereof is varied as compared to the length of the corresponding time interval for the output of the reference comparator, whereby the presence of said object can be
30 detected by detecting the condition where the outputs of the first mentioned comparator and reference comparator are not momentarily in the same state.



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- 5 16. An object detector as claimed in claim 15 wherein the first mentioned comparator and reference comparator are interconnected so as to synchronise the time of beginning of each cycle of the outputs thereof.
- 10 17. An object detector as claimed in claim 16 wherein the reference comparator is provided with second means for varying a said time interval for the output thereof, corresponding to the said time interval, the length of which is varied by influencing the rate of change and/or discharge of said capacitance.
- 15 18. An object detector as claimed in any one of claims 10 to 12 wherein the outputs of said free running multivibrator and said reference device are connected to switch means for producing an output when these outputs are not the same.
- 20 19. An object detector as claimed in any one of claims 15 to 18 wherein the outputs of said comparators are connected to switch means for producing an output when these outputs are not the same.
- 25 20. An object detector as claimed in any preceding claim wherein said first means is an electrode.
- 30 21. An object detector as claimed in claim 20 wherein said electrode is in the form of a coil.
22. An object detector as claimed in claim 12 or claim 17 wherein said first and second means comprise respective electrodes.



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23. An object detector as claimed in claim 22 wherein said electrodes are in the form of respective coils.

24. An object detector as claimed in any preceding claim wherein said capacitance at least includes a stray capacitance.

5 25. An object detector comprising an electronic switching device having an oscillator, two schmitt inverter gates, and means independently coupling the output of the oscillator to the inputs of both gates, said means independently coupling being effective to apply the output of the oscillator to the inputs of both gates during first
10 parts of cycles of the oscillator output signal, which first parts are of one polarity, and to decouple the oscillator from the inputs during second parts of cycles of the oscillator output signal, which second parts are of opposite polarity to said one parts, the inputs of the gates also being coupled to capacitances whereby the capacitances
15 discharge during application of said first parts of said cycles to the inputs of the gates, the capacitances charging during times when the output of the oscillator is decoupled from the inputs of the gates, the outputs of said gates changing polarity from first states thereof on application of said first cycle parts thereto and reverting
20 to said first state after cessation of said first cycle parts, after time periods necessary to bring the signal levels at the respective inputs of the gates to respective predetermined values by charging of said capacitors, which time periods are, in the absence of an object in the vicinity of the detector, dependant on the magnitude of
25 said capacitances, and wherein electrode means is provided which in use provides an electric field therearound and which is coupled to at least one said gate input whereby when a dielectric object is



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brought near said electrode means, the time period necessary to bring said signal level at at least one of said gate inputs to the respective predetermined level is varied relative to the corresponding time period for the other said gate input, and wherein means is provided
5 coupled to both gate outputs and responsive to a condition of change in the relative correspondence in switching times of the outputs of the gates from that prevailing when no object is near said electrode means, whereby in use of the detector the electric field is at least partially discharged in the presence of a said object near the elec-
10 trode means, to influence the rate of charging of the capacitances, and hence effect variations of said time periods, and so provide an indication of the presence of a said object near the electrode means.

26. An object detector substantially as herein described with reference to and as illustrated in Figs. 1 and 2, or Figs. 3 to 5,
15 or Figs. 6 and 7, or Fig. 6 as modified by Fig. 10, or Fig. 8, or Fig. 9 of the accompanying drawings.
