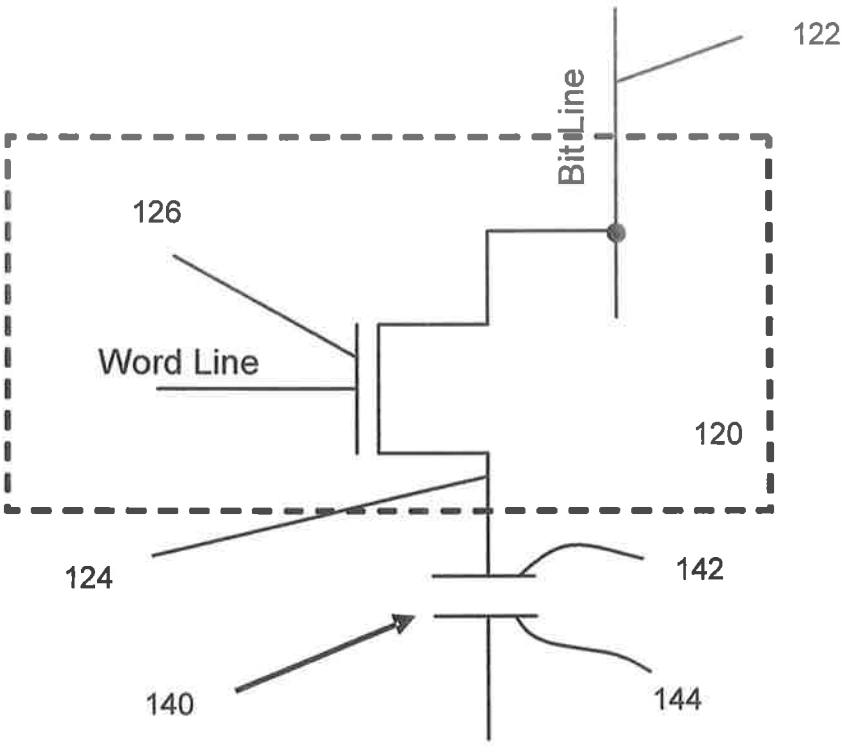
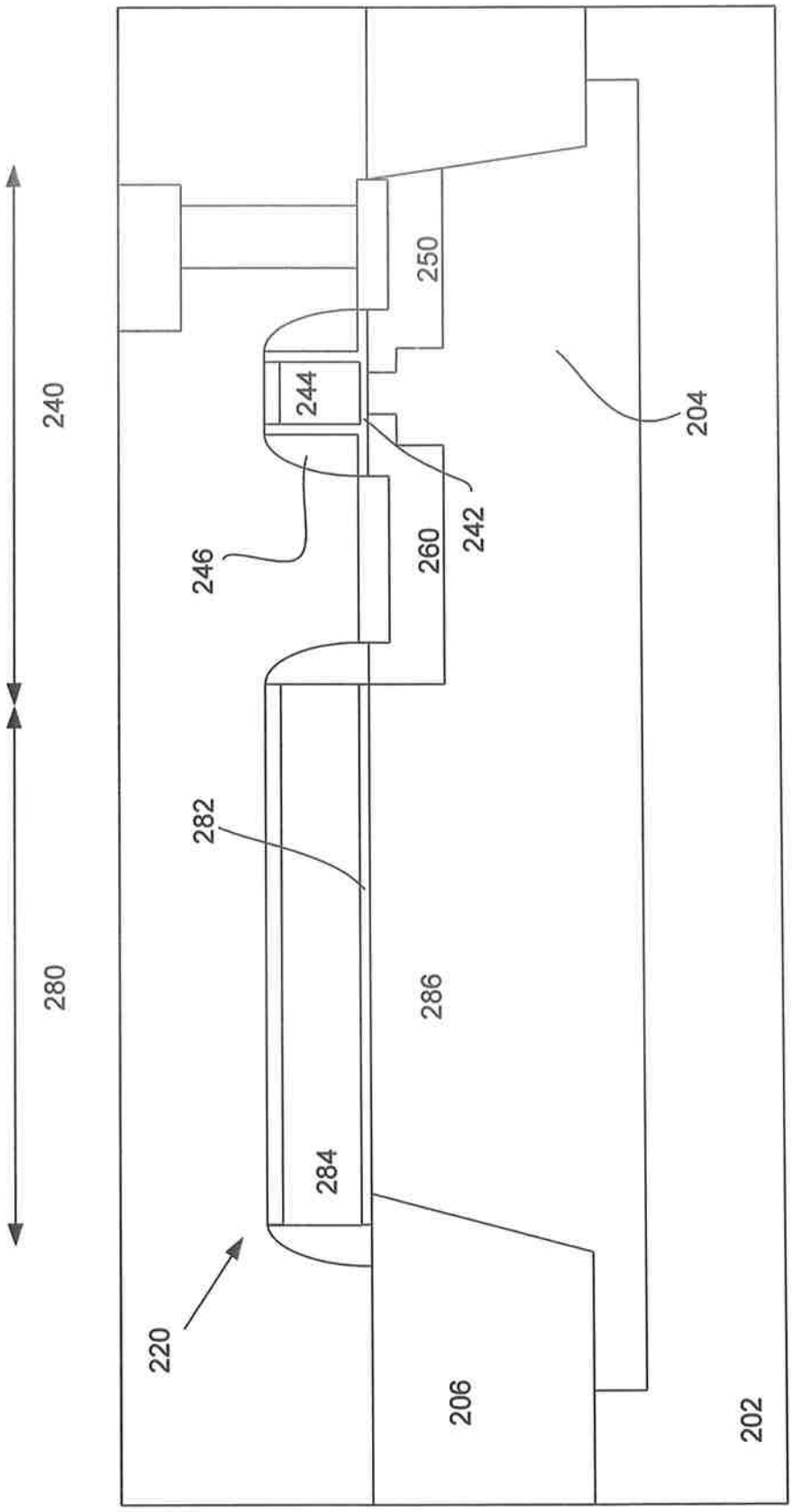


Prior Art

Figure 1



Prior Art

Figure 2

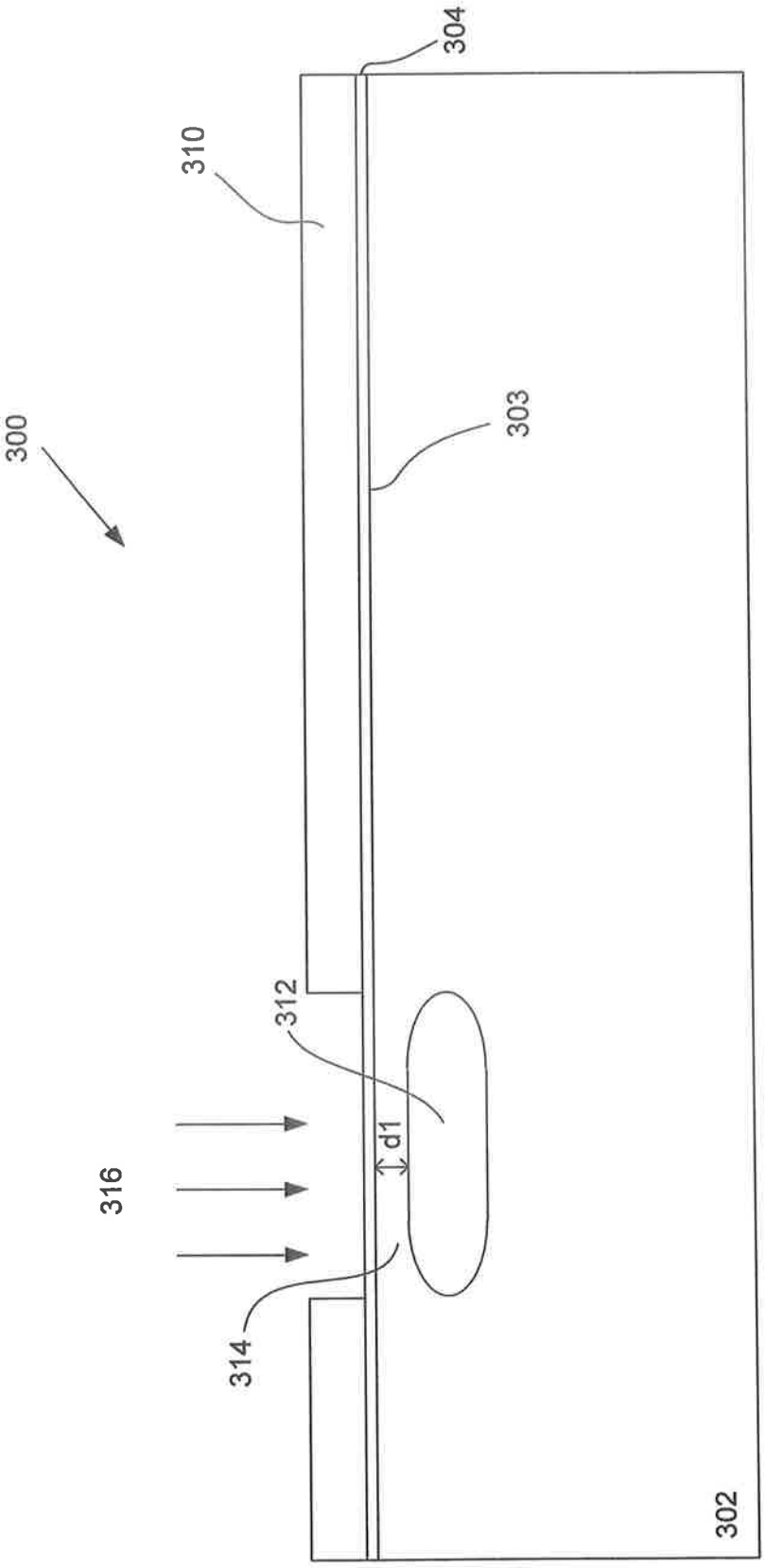


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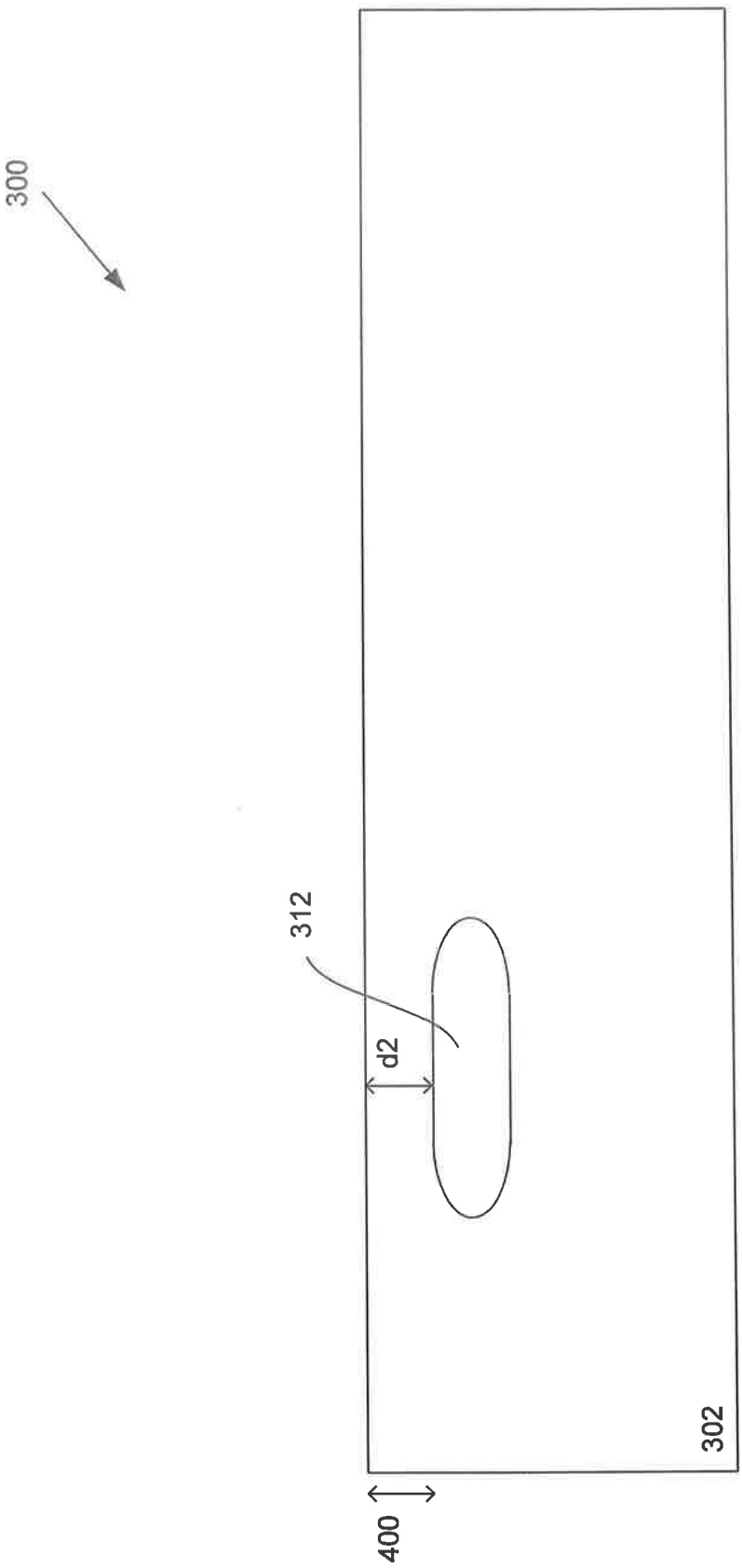


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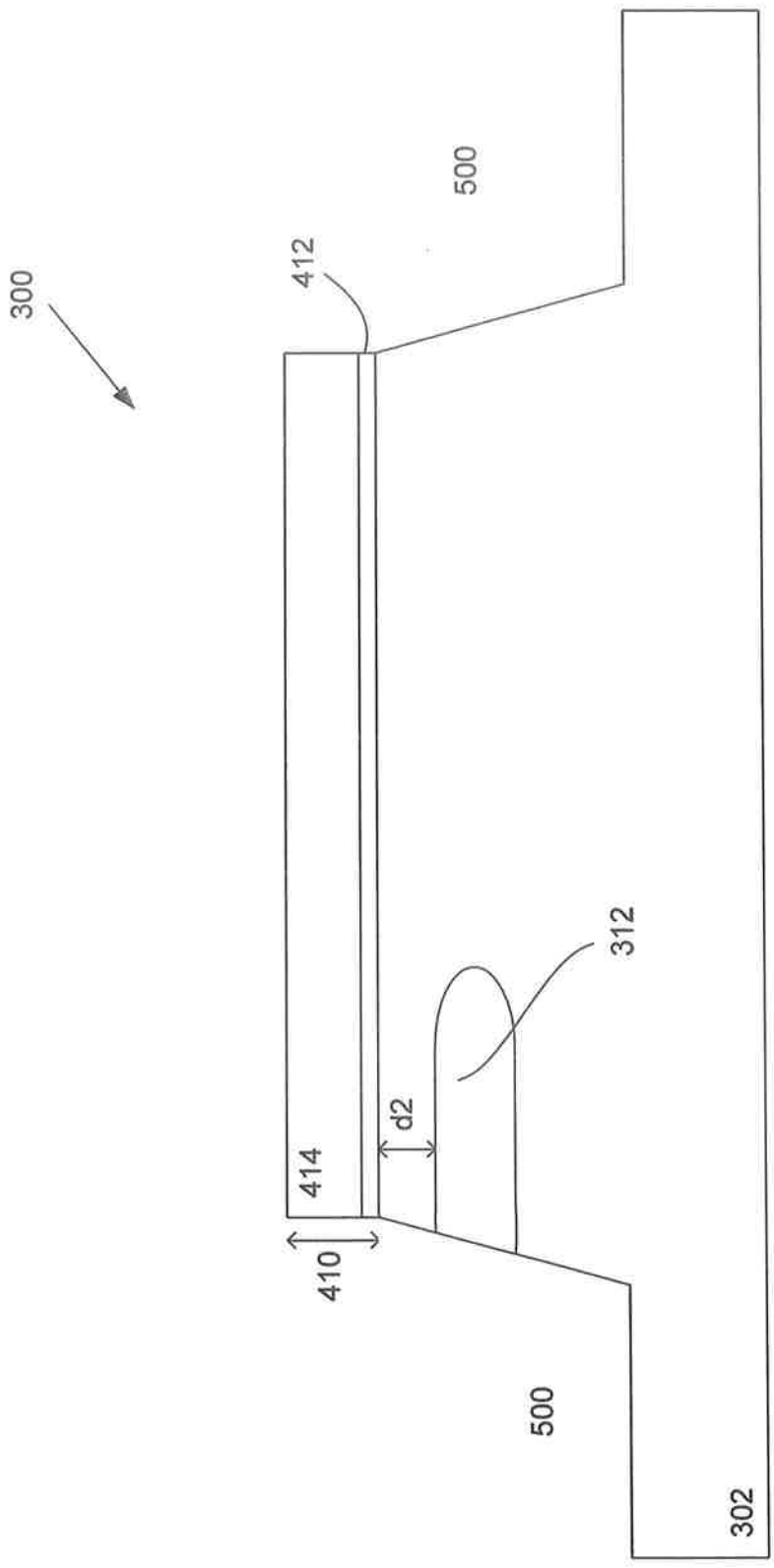


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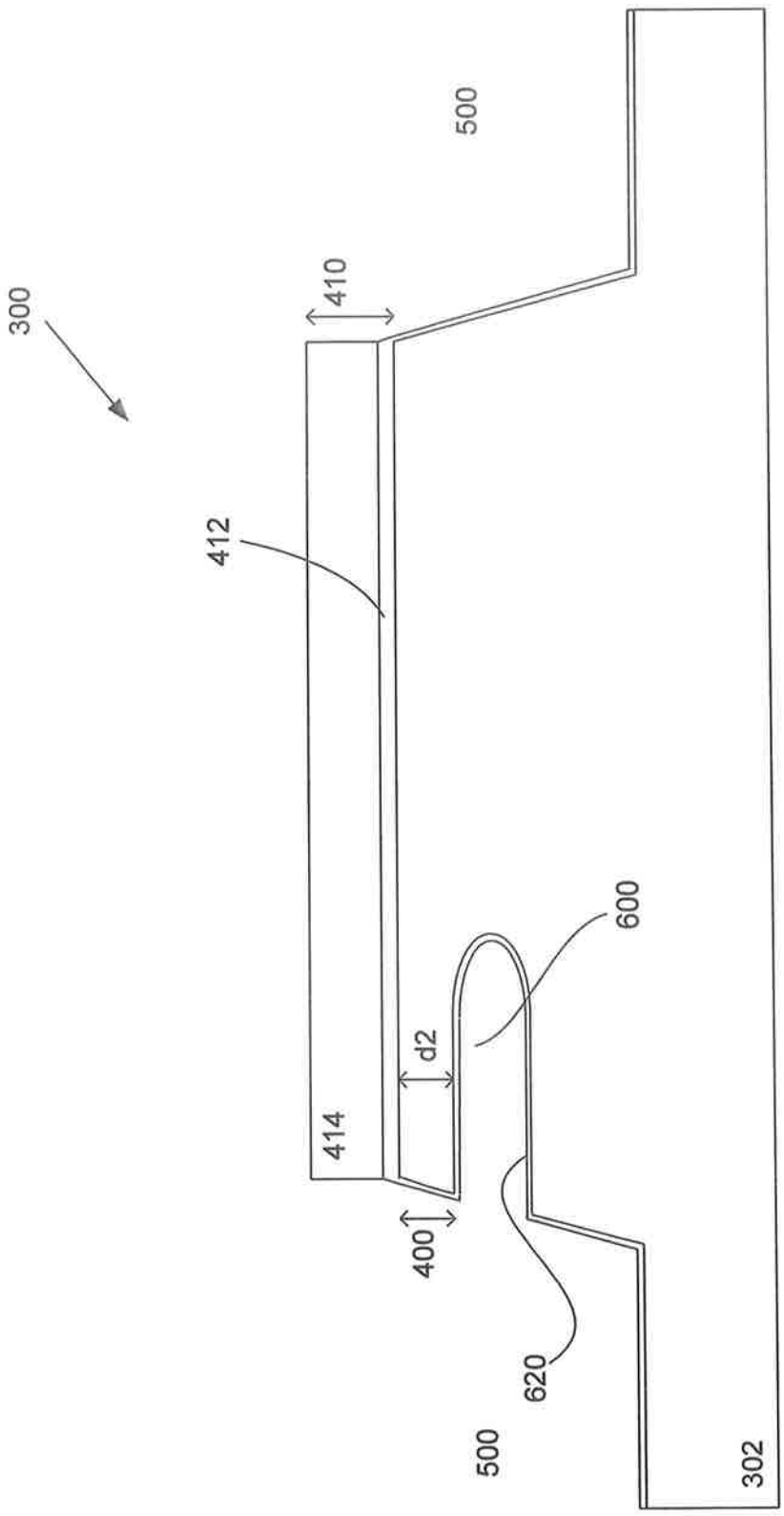


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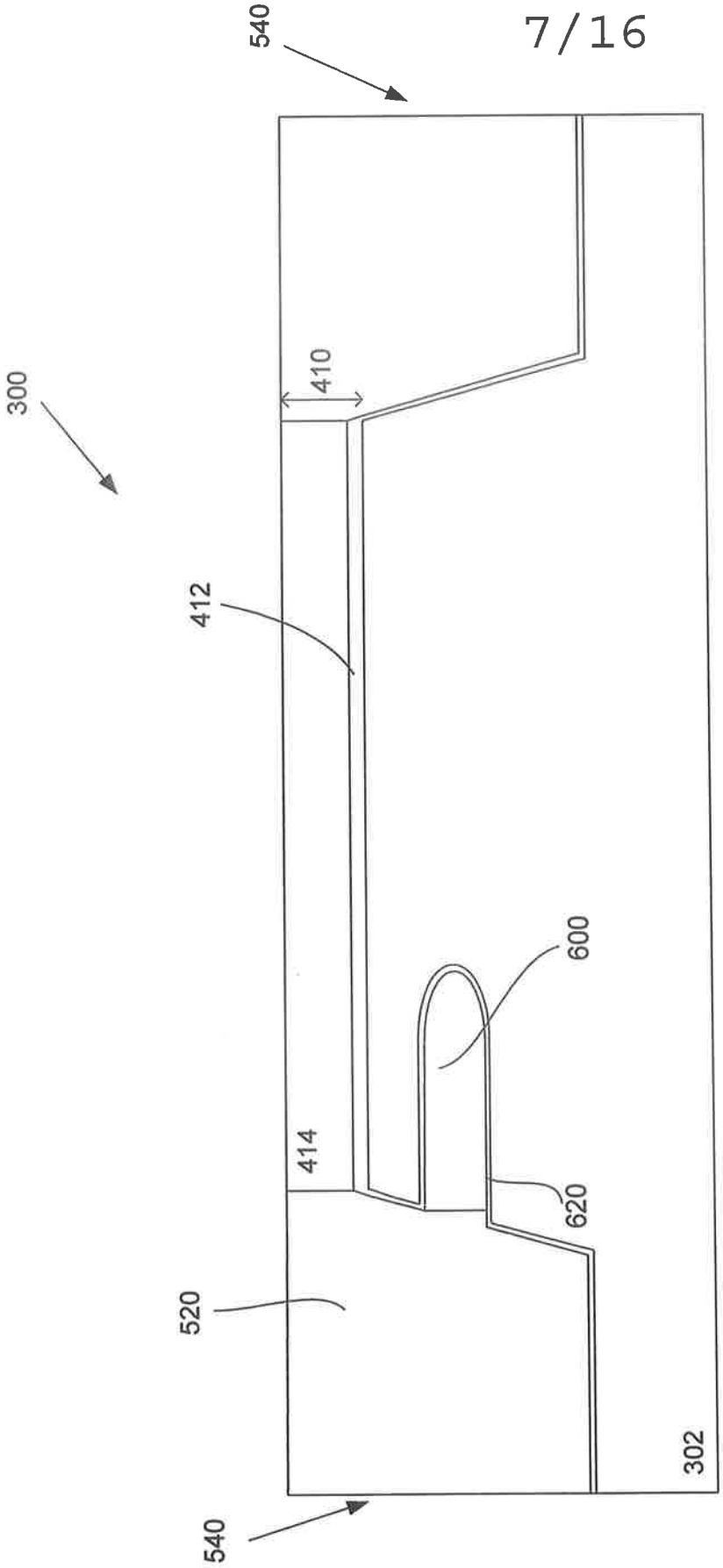


Figure 7

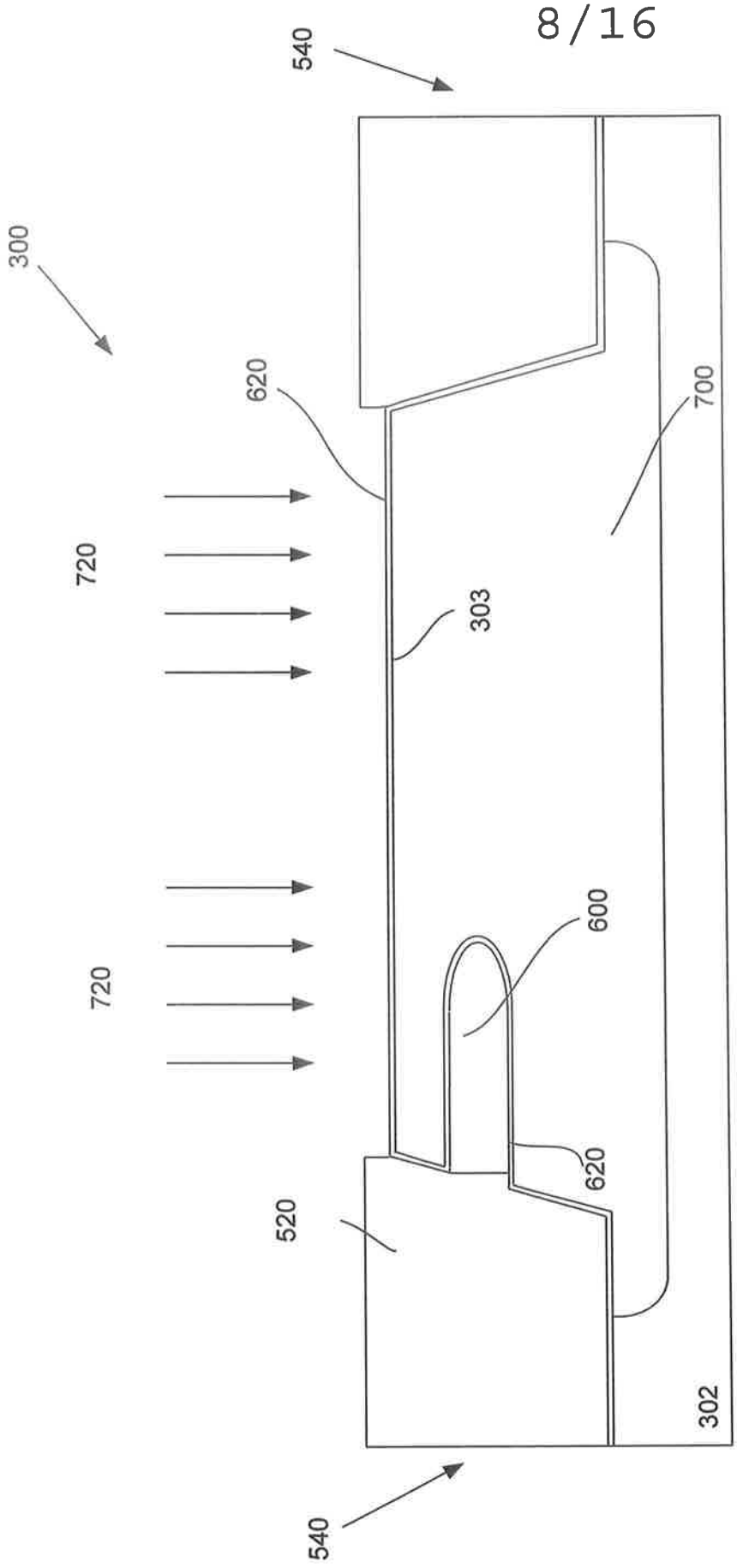


Figure 8

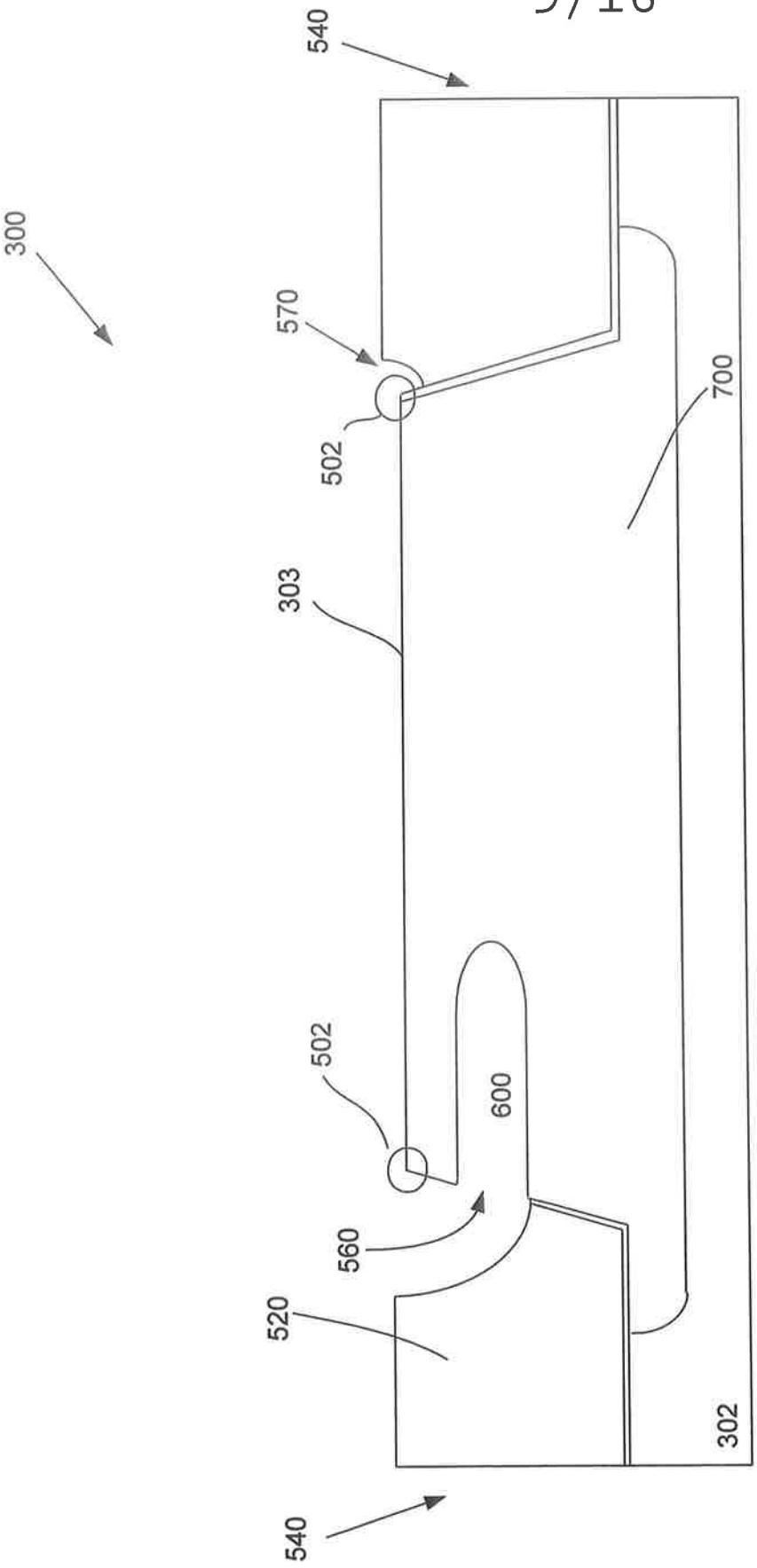


Figure 9

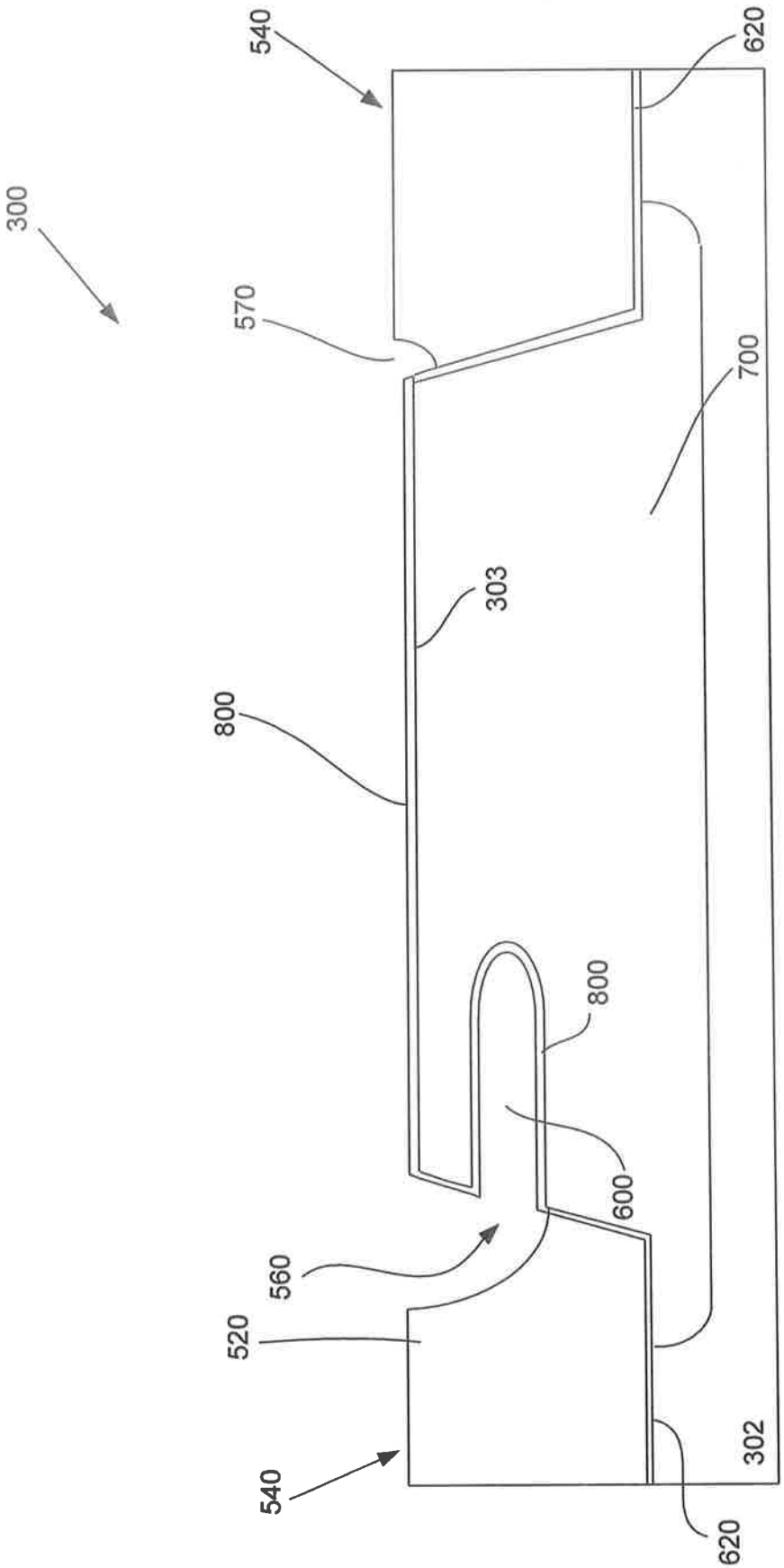


Figure 10

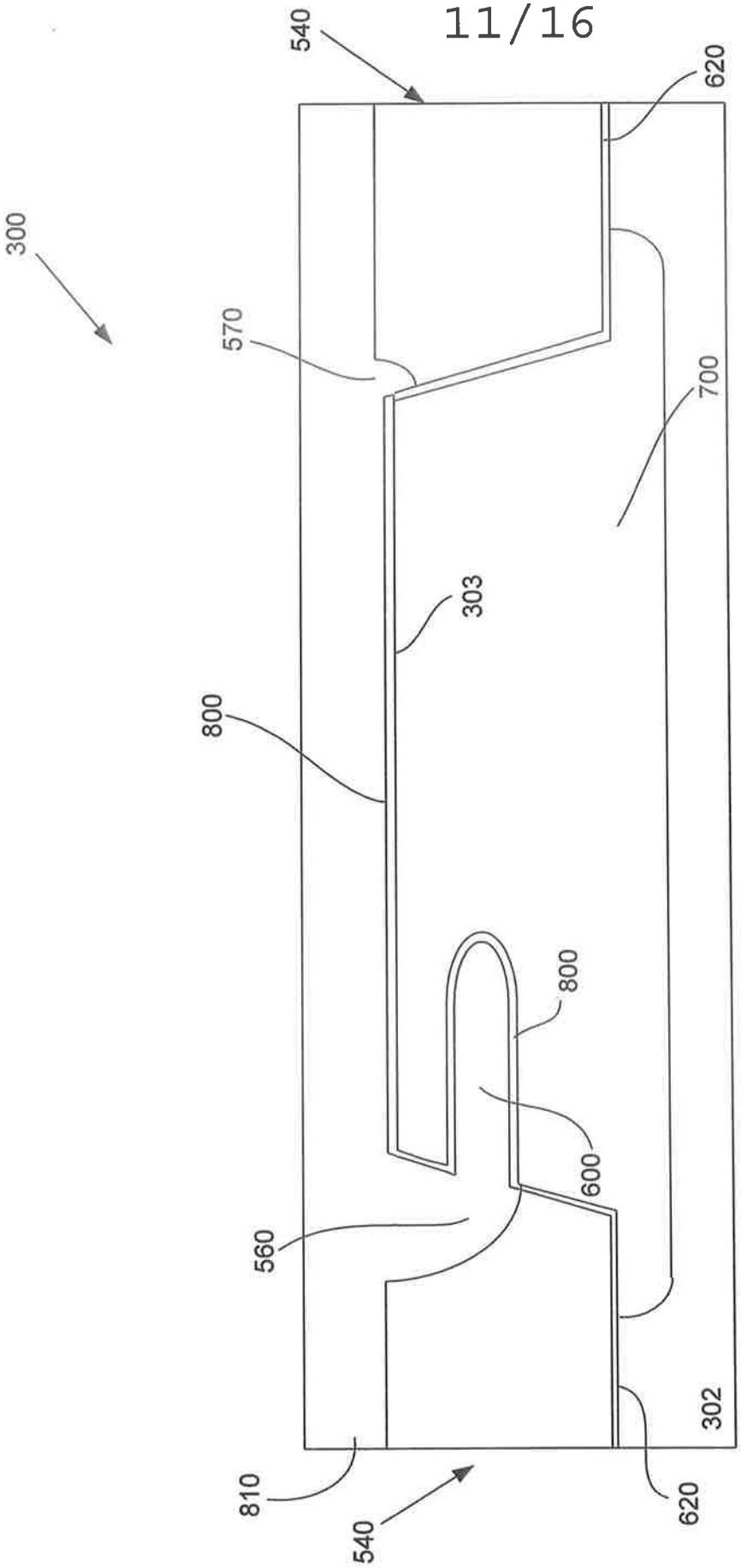


Figure 11

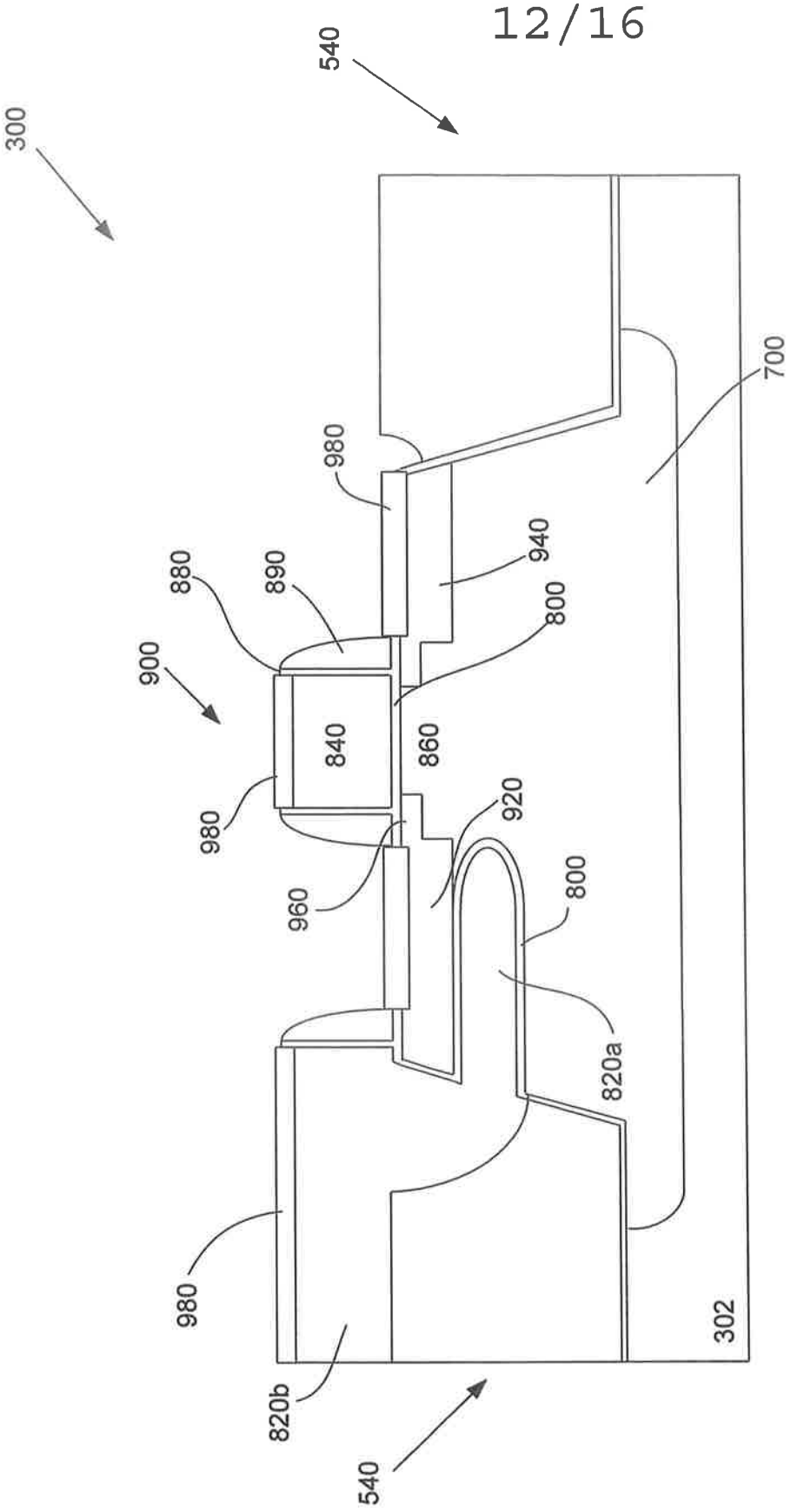

300
540
700
980
940
880
890
800
900
840
860
980
920
960
800
820a
980
820b
540
302

Figure 12

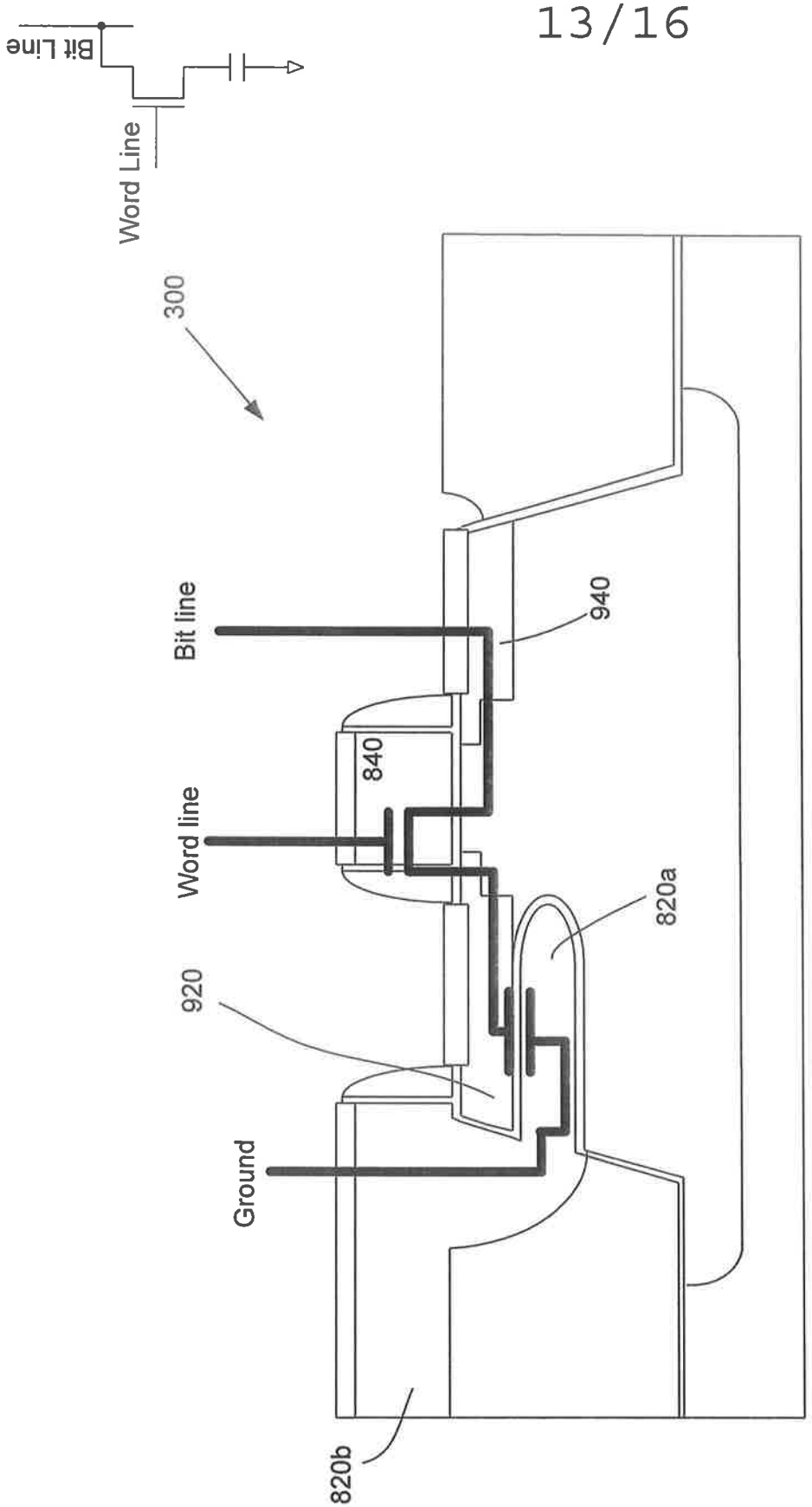

Bit Line
Word Line
300
Bit line
940
840
Word line
820a
920
Ground
820b

Figure 13

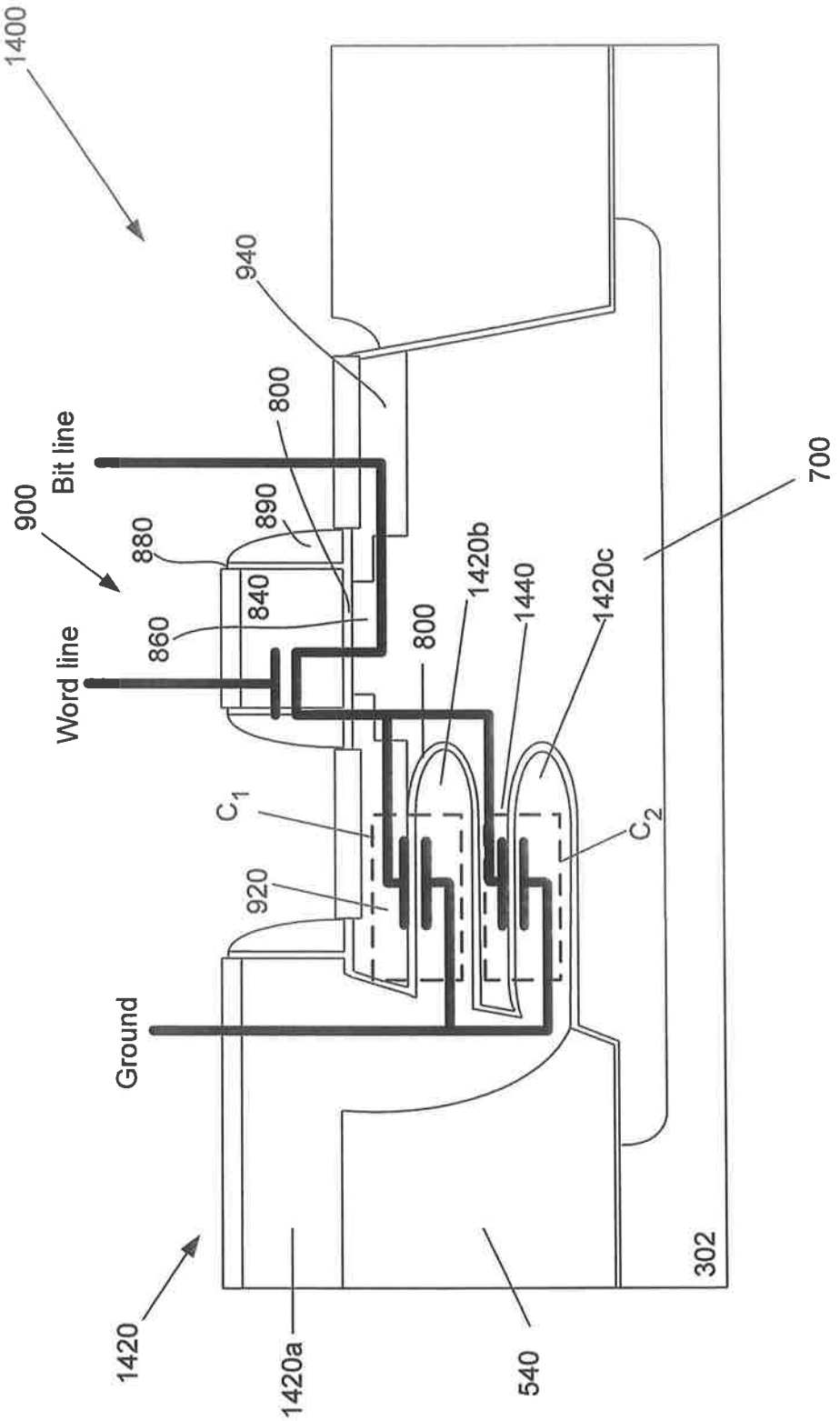

1400
940
800
Bit line
900
880
890
840
860
Word line
800
1420b
1440
1420c
700
C_1
C_2
920
Ground
1420
1420a
540
302

Figure 14

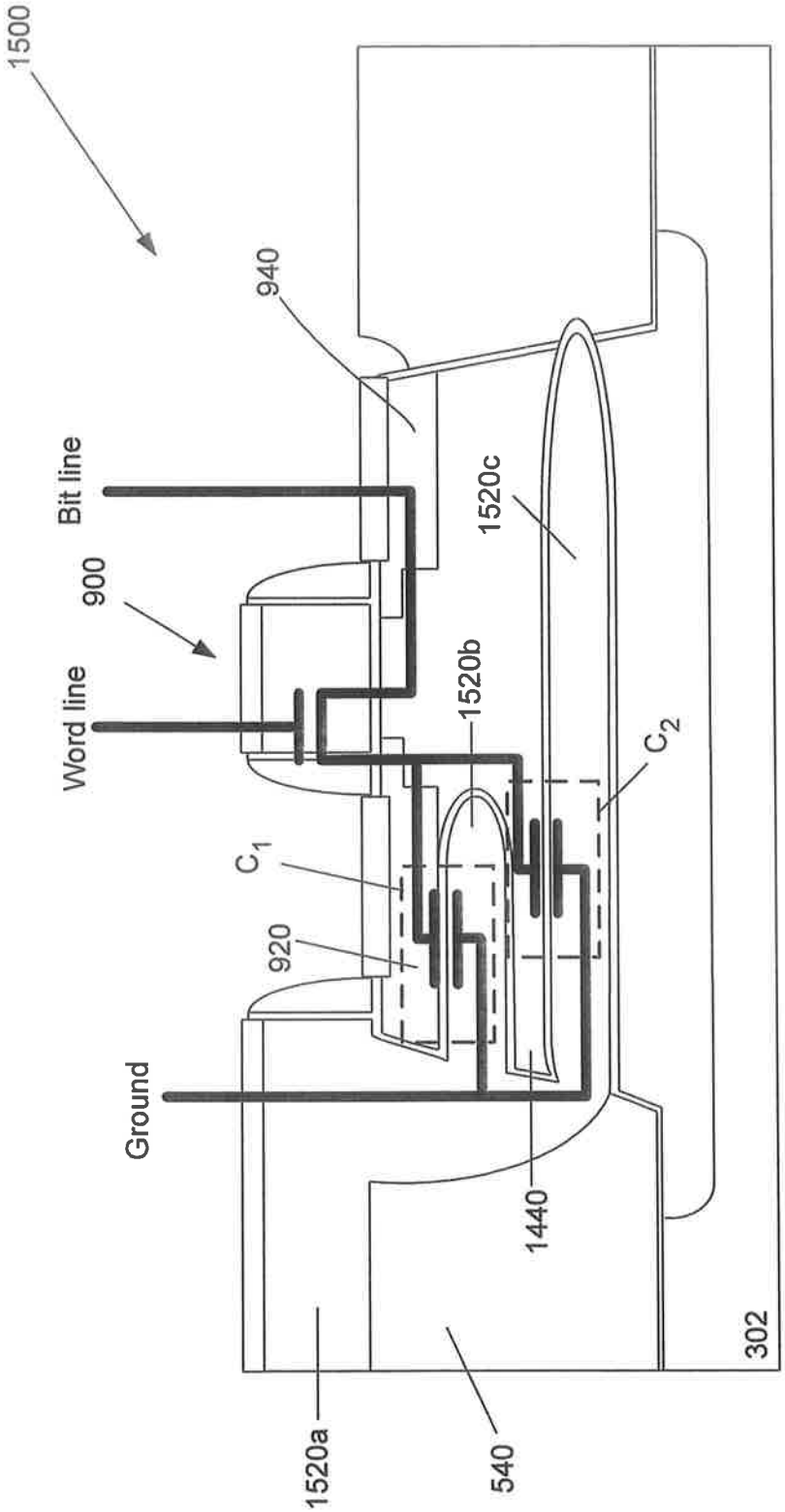

1500
940
Bit line
900
Word line
1520c
1520b
C_2
C_1
920
Ground
1440
302
1520a
540

Figure 15

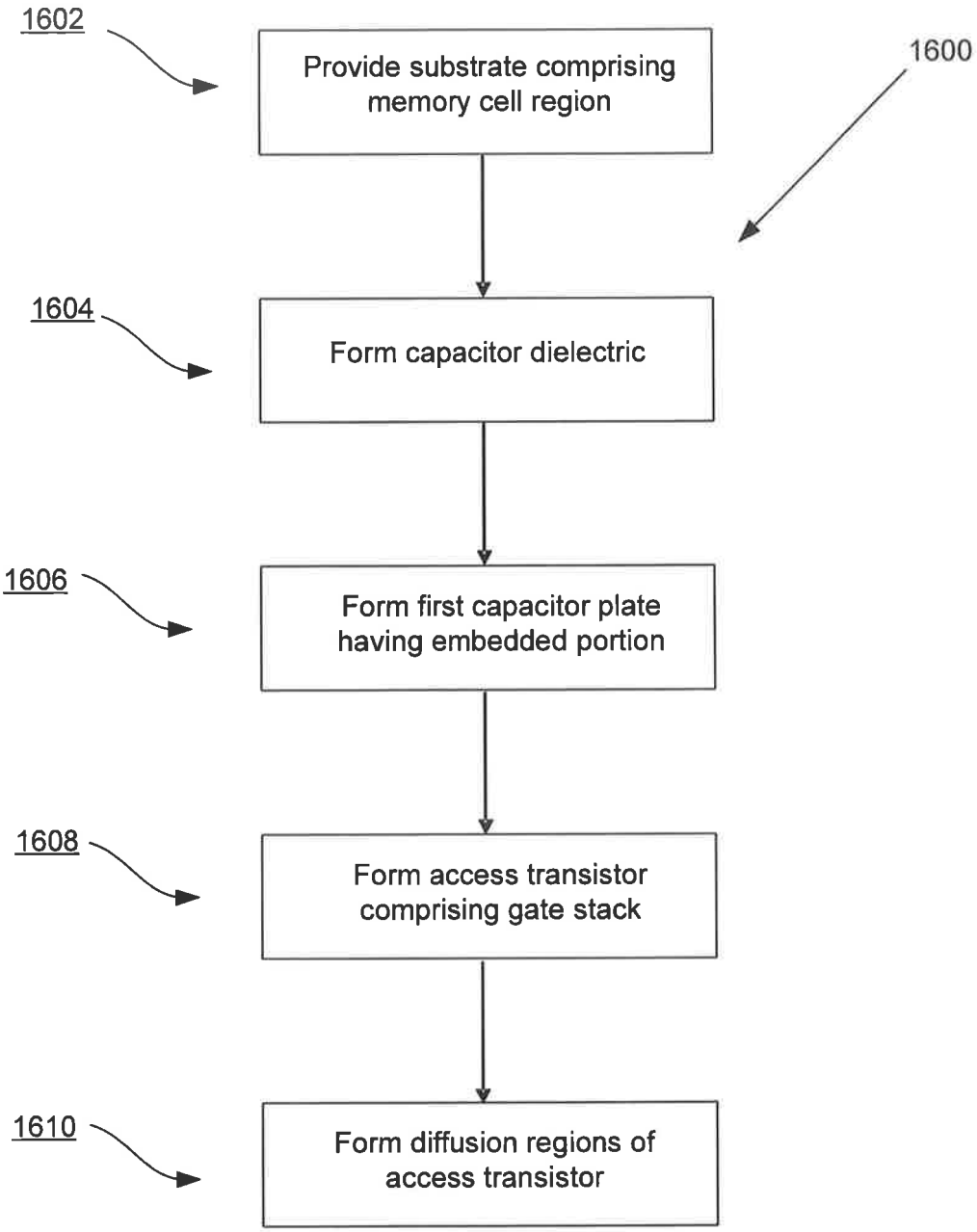

1602
Provide substrate comprising memory cell region
1600
1604
Form capacitor dielectric
1606
Form first capacitor plate having embedded portion
1608
Form access transistor comprising gate stack
1610
Form diffusion regions of access transistor

Figure 16