METHOD FOR BILAYER RESIST PLASMA ETCH

by Inventors,

Wendy Nguyen and Chris Lee

BACKGROUND OF THE INVENTION

[0001] The present invention relates to an improved method for plasma etching a bilayer resist in the fabrication of semiconductor devices.

[0002] The performance of today's integrated circuit chips is related to the dimensions of the transistors and wiring interconnects in the integrated circuits. As the dimensions of the transistors and wiring interconnects continue to shrink, the ability to pattern smaller features using photolithography has been a primary factor driving the success of the integrated circuit industry.

[0003] Photolithography processes involve the use of lithography imaging tools and photoresist materials. The minimum resolution achievable with the lithography imaging is governed by the minimum resolution for an exposure wavelength and a resolving power or numerical aperture of a lens system used by the lithography imaging tool. A shorter exposure wavelength for a larger numerical aperture often results in high resolution in order to print smaller patterns in a resist film. However, decreasing the wavelength or increasing the numerical aperture often results in a decrease in the depth of focus (DOF), thereby requiring the reduction and the thickness of the photoresist film.

[0004] Simply reducing the thickness of the resist film to enhance resolution is effective up to a certain point. This point is reached when the resist becomes too thin to withstand subsequent etching processes that transfer the resist pattern to one or more layers under the resist film. In order to overcome these problems, bi-layer resists have been developed to extend the photolithography technology. A bilayer resist film typically includes a relatively thick lower resist layer (also referred to as a masking or planarizing layer) disposed over a wafer or substrate, and a relatively thin upper resist layer, or imaging layer, disposed on top of the lower resist layer. The upper resist layer is patterned by light exposure and subsequently developed. The resulting upper layer pattern is used as a mask for etching the lower resist layer. In this way, a resist pattern with high aspect ratio can be formed in the bilayer resist film.

[0005] In order to provide sufficient etch resistance to the upper resist layer when the bilayer resist undergoes a lower resist layer etching process, silicon is typically incorporated into the

upper resist layer. Since the lower resist layer is typically made of organic polymers, an oxygen-based plasma is usually used to etch the lower resist layer, using the patterned top resist layer as a mask. Thus, while the lower resist layer is being etched in the oxygen based plasma, silicon precursors in the upper resist layer are oxidized to form a refractory oxide during the etching processes. The refractory oxide acts as an etch barrier, resulting in enhanced etching resistance of the upper resist layer. The enhancement achieved in this manner, however, is found in many applications to be insufficient.

[0006] The lower resist etching process not only requires good etch contrast between the upper resist layer and the lower resist layer, but also needs to be anisotropic to achieve good critical dimension (CD) control. With pure oxygen plasma, however, anisotropic etching can only be achieved when the temperature of the resist layers is maintained at or below about -100°C during the etching process. Otherwise, lateral etching or undercutting is usually observed indicating CD loss. Adding Sulfur dioxide (SO_2) to the oxygen based chemistry may be done in order to improve the anisotropic etching, however, lateral etching or undercutting still occurs at ambient temperature conditions. Additionally, the use of sulfur dioxide gas tends to cause corrosion of the equipment used for the lower resist layer etching process. Since sulfur dioxide is not typically used in conventional plasma processes, adding sulfur dioxide may require alteration of plasma processing equipment used in the conventional integrated circuit fabrication processes.

[0007] In view of the foregoing, there is a need for a method and apparatus to provide alternative anisotropic etching conditions when etching a bilayer resist.

SUMMARY OF THE INVENTION

[0008] Broadly speaking, the present invention fills these needs by introducing a scheme for providing anisotropic etching conditions for etching a bilayer resist. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, or a method. Several inventive embodiments of the present invention are described below.

[0009] A method for etching a bilayer resist defined over a substrate in a plasma etch chamber is provided. The method initiates with introducing the substrate having a pattern defined on a first layer of the bilayer resist into the etch chamber. Then, $SiCl_4$ gas flows into the etch chamber. Next, a plasma is struck in the etch chamber while flowing the $SiCl_4$ gas. Then the bilayer resist is etched.

[0010] A method of controlling critical dimension bias during a bilayer resist etch in an etch chamber is provided. The method initiates with striking an oxygen based plasma in a chamber while flowing $SiCl_4$ gas into the chamber. Then, a plasma density is maintained between about $1x10^9/cm^3$ and about $1x10^{12}/cm^3$. The bilayer resist is then etched.

[0011] It is to be understood that the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The accompanying drawings, which are incorporated in and constitute part of this specification, illustrate exemplary embodiments of the invention and together with the description serve to explain the principles of the invention.

[0013] Figure 1 is a schematic illustration of a stack of layers on a silicon substrate prior to forming a shallow trench isolation feature.

[0014] Figure 2 is a schematic illustration of a shallow trench etching process wherein the photoresist and BARC layers have been removed and the silicon nitride and pad oxide layers have been etched through.

[0015] Figure 3 is a schematic illustration of a shallow trench isolation feature etched into a silicon substrate.

[0016] Figure 4 is a photomicrograph of shallow trench isolation features having a bowed profile and subtrenched bottom.

[0017] Figure 5 is a photomicrograph of shallow trench isolation features etched with a silicon-containing gas.

[0018] Figure 6 is a photomicrograph of shallow trench isolation features which include top and bottom rounding.

[0019] Figure 7 is a schematic of a silicon substrate having a stack of layers thereon prior to carrying out a gate etch.

[0020] Figure 8 is a schematic illustration of a silicon substrate having silicon nitride and polysilicon layers thereon etched through to a gate oxide.

[0021] Figure 9A is a simplified schematic diagram of an etch profile without the use of a silicon containing gas in the etching gas mixture during the over etch step.

[0022] Figure 9B is a photomicrograph of an etched gate feature with CD control.

[0023] Figure 10 is a simplified cross sectional schematic diagram illustrating a dual doped gate structure that has been etched with a silicon containing gas utilized to mitigate etch rate differences caused by the dissimilar doping regions.

[0024] Figure 11 is a simplified schematic diagram of an etch chamber configured to provide a silicon containing gas during an over etch process.

[0025] Figure 12 is a simplified schematic diagram illustrating the various layers of a bilayer resist disposed over a substrate.

[0026] Figure 13A illustrates notching and undercutting occurring in the lower photoresist layer as a result of the use of silicon dioxide during the etching operation.

[0027] Figure 13B illustrates the elimination of the undercutting and notching with the employment of $SiCl_4$ gas introduced during the etch operation in accordance with one embodiment of the invention.

[0028] Figure 14A and 14B illustrate micrographs corresponding to Figures 13A and 13B illustrating the effectiveness of the use of $SiCl_4$ gas as compared to SO_2 in accordance with one embodiment of the invention.

[0029] Figure 15 is a flow chart diagram illustrating the method for etching a bilayer resist defined over a substrate in a plasma etch chamber in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] Several exemplary embodiments of the invention will now be described in detail with reference to the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention. Figures 1-11 discuss the use of silicon for shallow trench isolation etch applications and gate etching applications. Figures 12-15 discuss embodiments directed to the use of $SiCl_4$ for etching bilayer photoresists.

[0031] Many plasma etch applications rely on the generation of a passivation layer to obtain the desired feature profile. The primary mechanism for profile control involves the balance of etch and deposition reactions. The etch reactions are generally directly controlled by the reaction chamber parameters such as input power, pressure, and gas flows. In plasma etching of silicon

wafers, etch reaction products are the primary deposition source with the result that deposition mechanisms are indirectly controlled.

[0032] For shallow trench and gate applications, various etch gas chemistries are used. For example, when using HBr-O_2 etch gas chemistries, the passivation layer is primarily made up of $Si_xBr_yO_z$. For Cl_2-O_2 etch gas chemistries, the passivation layer is primarily made of $Si_xCl_yO_z$. Other constituents of the passivation layer can include N, C, H and F. Moreover, as a result of etching of silicon wafer and/or chamber materials such as quartz components, volatile silicon etch byproducts are incorporated into the passivation layer.

[0033] As explained above, silicon can be incorporated in passivation layers due to etching of silicon sources such as silicon wafers and/or chamber materials. Such silicon sources are secondary products that are not directly controlled by the etch gas chemistry. Moreover, as the volatile silicon etch byproducts are transported from the wafer surface toward the vacuum evacuation port, there is a finite possibility of deposition of the silicon-containing byproducts on the wafer surface. This can lead to non-uniform silicon byproduct concentration across the wafer and lead to non-uniformity of the etched feature profile and critical dimension.

[0034] The plasma may be produced in various types of plasma reactors. Such plasma reactors typically have energy sources which use RF energy, microwave energy, magnetic fields, etc. to produce a medium to high density plasma. For instance, a high density plasma could be produced in a transformer coupled plasma (TCP™) available from Lam Research Corporation which is also called inductively coupled plasma reactor, an electron-cyclotron resonance (ECR) plasma reactor, a helicon plasma reactor, or the like. An example of a high flow plasma reactor which can provide a high density plasma is disclosed in commonly owned U.S. Patent No. 5,820,261. The plasma can also be produced in a parallel plate etch reactor such as the dual frequency plasma etch reactor described in commonly owned U.S. Patent No. 6,090,304.

[0035] The process may be carried out in an inductively coupled plasma reactor maintained at a desired vacuum pressure by a vacuum pump connected to an outlet in a wall of the reactor. Etching gas can be supplied to a showerhead or injector arrangement by supplying gas from a gas supply to a plenum extending around the underside of a dielectric window. A high density plasma can be generated in the reactor by supplying RF energy from an RF source to an external RF antenna such as a planar spiral coil having one or more turns outside the dielectric window on top of the reactor. The plasma generating source can be part of a modular mounting arrangement removably mounted in a vacuum tight manner on the upper end of the reactor.

[0036] A wafer may be supported within the reactor on a substrate support such as a cantilever chuck arrangement removably supported by a modular mounting arrangement from a sidewall of the reactor. Such a substrate support is at one end of a support arm mounted in a cantilever fashion such that the entire substrate support/support arm assembly can be removed from the reactor by passing the assembly through an opening in the sidewall of the reactor. The substrate support may include a chucking apparatus such as an electrostatic chuck (ESC) and the substrate can be surrounded by a dielectric focus ring. The chuck may include an RF biasing electrode for applying an RF bias to the substrate during an etching process. The etching gas supplied by a gas supply may flow through channels between the window and an underlying gas distribution plate (GDP) and enter the interior of the chamber through gas outlets in the GDP. The reactor may also include a heated liner extending from the GDP.

[0037] The process may also be carried out in a parallel plate plasma reactor which includes an interior maintained at a desired vacuum pressure by a vacuum pump connected to an outlet in a wall of the reactor. Etching gas can be supplied to a showerhead electrode by supplying gas from a gas supply and a medium density plasma may be generated in the reactor by supplying RF energy from one or more RF sources to the showerhead electrode and/or a bottom electrode. Alternatively, the showerhead electrode may be electrically grounded and RF energy at two different frequencies can be supplied to the bottom electrode.

[0038] It will be apparent to those skilled in the art that the flow rates of the various gases will depend on factors such as the type of plasma reactor, the power settings, the vacuum pressure in the reactor, the dissociation rate for the plasma source, etc.

[0039] The reactor pressure is preferably maintained at a level suitable for sustaining a plasma in the reactor. In general, too low a reactor pressure may lead to plasma extinguishment, whereas in a high density etch reactor too high a reactor pressure can lead to the etch stop problem. For high density plasma reactors, the reactor is preferably at a pressure below 100 mTorr.

[0040] The substrate support supporting the semiconductor substrate undergoing etching preferably cools the substrate enough to prevent deleterious side reactions such as burning of any photoresist on the substrate and formation of undesirable reactant gas radicals. In high and medium high density plasma reactors, it is sufficient to cool the substrate support to a temperature of -10 to +80° C. The substrate support may include a bottom electrode for supplying an RF bias to the substrate during processing thereof and an ESC for clamping the substrate. For example, the substrate can comprise a silicon wafer which is electrostatically

clamped and cooled by supplying helium (He) at a desired pressure between the wafer and top surface of the ESC. In order to maintain the wafer at a desired temperature, the He may be maintained at a pressure of 10 to 30 Torr in the space between the wafer and the chuck.

[0041] Figure 1 - 3 show schematic representations of how a shallow trench may be etched into a silicon layer. As shown in Figure 1, a silicon substrate 10 includes a stack of layers thereon including a 100 Å pad oxide 12, a 1500 Å thick layer of silicon nitride 14, a 600 Å thick bottom antireflective coating (BARC) 16, and a 3200 Å thick layer of photoresist 18 which has been previously patterned to provide an opening 20. In etching shallow trenches on a silicon wafer, the photoresist 18 will include many openings 20 corresponding to the desired trench locations. The silicon nitride layer 14 is opened at the locations of the openings 20 to form a patterned hard mask.

[0042] In opening the hard mask 14, the BARC layer 16 is opened with a plasma etch. In an exemplary BARC open step, the chamber can be at a vacuum pressure of 5 mTorr and the antenna used to inductively couple radio frequency energy into the chamber can be set at 350 watts. The substrate support may include an electrode which provides an RF bias by powering the electrode with 88 watts. The BARC may be opened using a plasma etch with 50 sccm CF_4 for 60 seconds while maintaining the temperature of the wafer at about 60° C. Next, the silicon nitride layer 14 and pad oxide 12 are opened to form openings 22 with the chamber set at the same pressure but raising the antenna power to 1000 watts. The silicon nitride layer can be etched with 70 sccm CHF_3 and 300 sccm Ar for 44 seconds while maintaining the wafer temperature at about 60° C. After that, the photoresist and BARC are stripped using a chamber pressure of 10 mTorr and 1000 watts to the antenna. The photoresist may be stripped using 200 sccm O_2 for 45 seconds.

[0043] As a result of the strip step, the BARC and photoresist layer have been removed and areas of exposed silicon have become oxidized from the O_2 plasma. In an exemplary process, the chamber is set at 5 mTorr and 350 watts power is supplied to the antenna. The oxidized silicon is etched using 50 sccm CF_4 for 7 seconds while maintaining the wafer temperature at about 60° C. Next, the silicon substrate may be etched with the chamber pressure set at 50 mTorr and 1000 watts power being supplied to the antenna. The bottom electrode may be supplied about 220 watts power and the etch gas can include 125 sccm Cl_2, 14 sccm O_2 and 14 sccm N_2 while maintaining the wafer temperature at about 60° C. In order to provide desired rounding and/or profile and/or CD control, a silicon containing gas such as $SiCl_4$ can also be

added to the etch gas. After forming the trench structure 24 as shown in Figure 3, the wafer can be cleaned using a 2 minute HF dip followed by a deionized water spin rinse.

[0044] Figure 4 is a photomicrograph of a trench structure formed using 125 sccm Cl_2 and no $SiCl_4$ addition to the etch gas. As shown in Figure 4, the trenches have a bowed profile and subtrenched bottoms. Improved critical dimension (CD) and profile control can be obtained by adding a silicon-containing gas to the etch gas. Figure 5 is a photomicrograph of a trench structure formed when a silicon-containing gas is used during the shallow trench etch. The trench structure shown in Figure 5 was etched with 75 sccm Cl_2 and 25 sccm $SiCl_4$. Figure 6 is a photomicrograph of tapered trenches having rounded tops and bottoms as a result of using a silicon-containing gas during the shallow trench etch.

[0045] Figures 7 and 8 are schematics representative of a gate etch. As shown in Figure 7, a silicon wafer 30 includes a stack of layers thereon which includes a 15 Å thick layer of oxide 32, a 1500 Å thick layer of polysilicon 34, a 200 Å thick layer of silicon nitride 36, and a 2000 Å thick layer of photoresist 38, which has been patterned to include openings 40 therein corresponding to the locations of the gate etch. It should be appreciated that the barrier layer is not limited to silicon nitride. For example, one skilled in the art will appreciate that the hardmask in gate application is silicon dioxide (SiO2) or silicon oxynitride (SiOxNy). In addition, the thickness of the barrier layer may be 300 Å, or any other suitable thickness. While a single opening 40 is shown in Figure 7, in etching gate structures on a wafer there will be many openings 40 corresponding to the desired locations of the gates.

[0046] An exemplary process of a gate etch is as follows. Initially, a trimming step is carried out with the chamber pressure set at 15 mTorr and the antenna power set at 400 watts. The etch gas for the trimming step can include 30 sccm HBr and 10 sccm O_2. Then, the silicon nitride layer 36 is etched with the chamber set at 10 sccm CF_4 to provide an opening in the silicon nitride layer 36 corresponding to the opening 40. Then, the polysilicon is etched in four steps which includes a breakthrough step, a first main etch, a second main etch and an over etch. In the breakthough step, the native oxide present at the surface of the silicon is etched because some chemistries, e.g., HBr, do not etch the SiO_2 easily or uniformly. It will be apparent to one skilled in the art that where the chemistry contains CF_4, the use of a breakthrough step is not necessary. In the first main etch, the chamber is set at 10 mTorr and the antenna is set at 800 watts power. The etch gas includes 50 sccm Cl_2, 175 sccm HBr, 60 sccm Cf_4 and 5 sccm O_2. In the second main etch, the chamber is set at 30 mTorr and the antenna is set at 350 watts. The etch gas for the second main etch includes 300 sccm HBr and 3 sccm O_2. In the over etch, the

chamber is set at 80 mTorr and the antenna is supplied 500 watts power. The etch gas in the over etch includes 130 sccm HBr, 4 sccm O_2 and about 270 sccm He. A silicon containing gas such as $SiCl_4$ can be added to the first or second main etch and/or the over etch to improve gate profile control and within wafer CD control. After the polysilicon etch, an opening 42 extends to the gate oxide 32, as shown in Figure 8.

[0047] Figure 9A is a simplified schematic diagram of an etch profile without the use of a silicon containing gas in the etching gas mixture during the over etch step. Etched gate feature 102a through 102c include notches 100 at the base of each of the etch-gate features. As preserving the gate integrity at the end of the etch process when polysilicon stringers are removed, i.e., during the over-etch step, high selectivity to the oxide needs to be maintained while performing the over-etch step. As is generally known, gate oxide pitting is a phenomenon by which the gate oxide, or the gate material, is etched selectively in small localized areas resulting in etching of the silicon underneath, thereby creating pits.

[0048] Figure 9B is an exemplary photomicrograph of an etched gate feature with critical dimension control obtained by adding a silicon containing gas to the over-etch process in accordance with one embodiment of the invention. Silicon-containing gas in the silicon etching gas mixture increases the amount of sidewall passivation in order to mitigate any notching. Thus, gate feature 102a through 102c are shown having a notch-free base due to the sidewall passivation provided by the addition of silicon-etching gas. In one embodiment, with respect to hard mask gate applications, the sidewall passivation mainly consists of a Si, O, X-based material with X being a halogen or a mixture of halogens, e.g., bromine, chlorine, fluorine, etc. One skilled in the art will appreciate that the halogen may be dependent on the etch chemistry. Here, the first two etch steps incorporate silicon into the passivation layer from the substrate through reactions involving etch byproducts. However, at the end of the polysilicon etch, during the over-etch step, the silicon-based byproducts are depleted due to the depletion of silicon material to be etched. At the same time, the etching species concentration is increased. As a result, little passivation is created during the over-etch step and the existing passivation at the base of the line can be attacked by the etching species resulting in notching of the polysilicon line. However, the addition of silicon during the over-etch step will replace the depleted silicon previously supplied by the silicon material being etched.

[0049] Figure 10 is a simplified cross sectional schematic diagram illustrating an etched dual doped gate structure. Here, gates 110 are composed of n-doped polysilicon, while gate 112 is composed on p-doped polysilicon. It should be appreciated that adding a silicon containing gas

during the entire etch process enhances the formation of a passivation layer, thereby mitigating differences caused by the dissimilar doped gate structures on the substrate. The amount of the lateral attack can also vary with the doping type during the last steps of the gate-etch process when the etch chemistry becomes more selective to the gate oxide. Consequently, the profiles defined in the first step of the silicon etch may be altered in the final steps, leading to profile and critical dimension differences between the various doped regions, i.e., also referred to as n/p profile loading. Thus, in another embodiment, the addition of a source of silicon on a gas mixture in the last steps of the etch, e.g., the over-etch step, decreases the etch rate micro-loading between different types of doped silicon. In addition, the silicon gas adds more passivation to the lines, thereby reducing the impact of the lateral etch differences between the various types of doped silicon on the profile definition.

[0050] Accordingly, adding a silicon-containing gas in the etch gas mixture during the silicon etch will eliminate the notching at the base of the features. Additionally, the silicon-containing gas in the etch-gas mixture during the over etch step will increase the selectivity to oxide. Furthermore, a silicon-containing gas in the etch gas mixture during the silicon etch will reduce the profile differences between the various type of doped silicon present on the same substrate. That is, adding a silicon-containing gas in the etch gas mixture during the silicon etch will reduce the critical dimension bias differences between n-doped, p-doped or undoped lines.

[0051] Figure 11 is a simplified schematic diagram of an etch chamber configured to provide a silicon containing gas during an over etch process. Etch chamber 120 includes gas inlet 122, top electrode 124, electrostatic chuck 128 supporting wafer or semiconductor substrate 126. Etch chamber 120 also includes outlet 130 which may be in flow communication with a pump for evacuating the etch chamber. Process gas supply 132 is in flow communication with gas inlet 122. It should be appreciated that a passivation enhancing gas, e.g., a silicon containing gas as mentioned above, may be provided to the chamber through gas inlet 122. Controller 134, which is in communication with chamber 120 and process gas supply 134, may be configured to detect a passivation starved condition, i.e., an over etch process. In response to detecting the passivation starved condition, the controller may trigger process gas supply 134 to supply a silicon containing gas to chamber 120. It should be appreciated that controller 134 may detect the passivation starved condition through any suitable endpoint detection or the start of the over etch process may trigger the supply of the silicon containing gas. Furthermore, controller 134 is a general purpose computer in one embodiment.

[0052] The parameters associated with the introduction of the silicon containing gas, e.g., $SiCl_4$ are summarized in TABLE 1.

TABLE 1

Pressure	0.5-200 mTorr
Power	10-5000 W
$SiCl_4$ flow	0.1 – 300 sccm
Temperature	-77 C to 200 C

It should be appreciated that TABLE 1 is exemplary and not meant to be limiting. That is, any suitable silicon containing gas may be used. Furthermore, depending on the chamber configuration, the range of parameters may vary.

[0053] In one embodiment, when $SiCl_4$ or another suitable Si containing gas is added to the gas mixture in the over etch step, the polysilicon is still etched, however, a protective deposition takes place on the gate oxide. That is, a thin layer of SiO_x, which may incorporate Br or Cl or any other suitable element present in the chamber, is deposited on the gate oxide or nitridized gate oxide. It should be appreciated that a source of oxygen is also provided to form the SiO_x layer. The oxygen source for the thin layer may originate from the introduction of an oxygen containing gas or the presence of an oxygen containing component in the vessel, e.g., quartz, alumina, an oxygen containing component of the substrate being etched, etc. It should be appreciated that the etch rate selectivity between polysilicon and oxide becomes infinite, i.e., there is no etching of the gate oxide, as a result of the deposition of the thin silicon containing oxide layer. Consequently, this results in improved gate integrity, i.e., minimal if any oxide loss, less silicon recess and significantly reduces the chances of pitting. Furthermore, the increased etch rate selectivity widens the process window since the process may operate in a region where pitting would otherwise occur without the improved selectivity.

[0054] In another embodiment, a solid source of silicon may be included in the chamber in order to provide the silicon for the passivation layer. That is, during an over etch process where the silicon being etched is substantially depleted, the solid source of silicon provides the silicon required for the passivation layer in order to prevent notching. For example, a top electrode of the etching chamber may include the solid silicon source, which may be triggered during the over etch step by applying a radio frequency (RF) bias to the top electrode.

[0055] Table 2 illustrates the processing parameters associated with an etching chamber in order to achieve the embodiments described herein with reference to anisotropic etching conditions for etching a bilayer resist. It should be appreciated that Table 2 is exemplary and not meant to be limiting. The parameters listed in Table 2 were employed with the use of a Versys 2300 etching machine available from the assignee. Of course, the ranges listed in Table 2 may vary according to the type of machine performing the etch operation.

TABLE 2

Pressure	0.5-200 mTorr
Top Power	10-5000 W
Bottom power	200-300 V_{pk}
Temperature	20 C to 70 C
$SiCl_4$ flow	0.1 – 6 sccm
O_2 flow	100-200
N_2 flow	50 – 200 sccm
Cl_2 flow	10 – 50 sccm
HBr flow	50 – 100 sccm

[0056] With respect to the gases employed during the bilayer resist etch, one suitable combination includes the use of oxygen (O_2), nitrogen (N_2), $SiCl_4$, Hydrogen Bromide (HBr), and chlorine (Cl_2). A range for the flow rate of oxygen is approximately 100 - 200 standard cubic centimeters per minute (sccm). Here, oxygen is used as the etchant. The flow rate of nitrogen during the processing is between about 50 and 200 sccm. It should be appreciated that nitrogen assists with maintaining consistency across the substrate surface. An exemplary flow rate for hydrogen bromide is between about 50 and 100 sccm. The hydrogen bromide is used for sidewall passivation. The chlorine flow rate is between about 10 and 50 sccm. In one embodiment, the chlorine flow rate is approximately 10% of the oxygen flow rate. That is, the ratio of the oxygen flow rate to the chlorine flow rate is 10:1. Chlorine is employed to help remove volatile gases. The $SiCl_4$ flow rate is between 0.1 and 6 sccm. The $SiCl_4$ gas is used to help maintain CD in accordance with the embodiments described herein.

[0057] Other settings used during the bilayer resist etch include a pressure range between about 3 and 15 milliTorr (mTorr). The power to an upper electrode is between about 300 to 1000 watts, while the peak power available to a bottom electrode is between about 200 and 300 volts.

The chamber temperature is between about 20 to 70 degrees Celsius as shown in Table 2. In one embodiment, the plasma density is maintained between $1x10^9$ per cubic centimeter and $1x10^{12}$ per cubic centimeter. The settings of pressure and top power illustrated in Table 2 define this plasma density. Ion energy is maintained between about 150 and about 400 volts, where the ion energy is a function of the RF peak power supplied to the bottom electrode.

[0058] Figure 12 is a simplified schematic diagram illustrating the various layers of a bilayer resist disposed over a substrate. Here, wafer 150 includes polysilicon layer 152, bottom photoresist layer 154 and top photoresist layer 156. Top photoresist layer 156 is subsequently patterned and developed. Thereafter, the bilayer photoresist, which consists of first photoresist layer 154 and second photoresist layer 156, is etched to define a pattern. Typically, top photoresist layer 156 includes silicon, while bottom photoresist layer is an organic photoresist.

[0059] Figures 13A and 13B illustrate a pattern defined through an etch of the bilayer photoresist when using standard poly-silicon chemistry and $SiCl_4$ gases, respectively. Figure 13A illustrates notching and undercutting occurring in the bottom photoresist layer 154 as a result of conventional chemistry during the etching operation. As shown in Figure 13A there is a loss of the critical dimension defined between the etched bottom photoresist layers 154 due to the notching and undercutting, which in turn will impact the subsequent etching of polysilicon layer 152. However, Figure 13B illustrates the elimination of the undercutting and notching with the utilization of $SiCl_4$ gas introduced during the etch operation. Here, the etching of bottom photoresist layer 154 and top photoresist layer 156 results in an etch operation that does not lose CD.

[0060] Figure 14A and 14B illustrate actual micrographs corresponding to Figures 13A and 13B illustrating the effectiveness of the use of $SiCl_4$ gas in accordance with one embodiment of the invention. As shown in Figure 14B, the loss of CD is minimal as compared to Figure 14A. Figure 14A was the result of using standard polysilicon chemistry (HBr, O_2, N_2) during the etch operation. Figure 14B utilized Cl_2, HBr, O_2, N_2, and $SiCl_4$ gases for the etch operation. It should be appreciated that the $SiCl_4$ forms SiO_2 with the O_2 during the etch operation in order to minimize the loss of CD.

[0061] Figure 15 is a flow chart diagram illustrating the method for etching a bilayer resist defined over a substrate in a plasma etch chamber in accordance with one embodiment of the invention. The method initiates with operation 160 where a substrate having a pattern defined on a first layer of a bilayer photoresist is introduced into an etch chamber. The method then advances to operation 162 where $SiCl_4$ gas flows into the etch chamber, along with the mixture

of gases listed in Table 2. As described with reference to Table 2 the flow rate of the $SiCl_4$ gas is between 0.1 and 6 SCCM in one embodiment. The method then proceeds to operation 164 where an oxygen based plasma is struck in the etch chamber while flowing the $SiCl_4$ gas into the chamber. Here, the gases listed with reference to Table 2 flow into the chamber along with the $SiCl_4$ gas. In one embodiment, a plasma density of between about $1x10^9$ per cubic centimeter and $1x10^{12}$ per cubic centimeter is maintained in the etch chamber. In another embodiment, an ion energy of between about 150 volts and about 400 volts is maintained in the etch chamber. The method then moves to operation 166 where the bilayer resist is etched according to the conditions described herein.

[0062] The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as being limited to the particular embodiments discussed. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those embodiments by one skilled in the art without departing from the scope of the present invention as defined by the following claims.

[0063] The invention has been described herein in terms of several exemplary embodiments. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention. The embodiments and preferred features described above should be considered exemplary, with the invention being defined by the appended claims.

What is claimed is:

CLAIMS

1. A method for etching a bilayer resist defined over a substrate in a plasma etch chamber, comprising method operations of:

introducing the substrate having a pattern defined on a first layer of the bilayer resist into the etch chamber;

flowing $SiCl_4$ gas into the etch chamber;

striking a plasma in the etch chamber while flowing the $SiCl_4$ gas; and

etching the bilayer resist.

2. The method of claim 1, wherein the method operation of flowing $SiCl_4$ gas into the etch chamber includes,

flowing the $SiCl_4$ gas at a flow rate between about 0.1 standard cubic centimeters per minute (sccm) and 6 sccm.

3. The method of claim 1 further comprising:

flowing chlorine gas into the etch chamber;

flowing hydrogen bromide gas into the chamber; and

flowing an inert gas into the chamber.

4. The method of claim 3, wherein the inert gas is nitrogen.

5. The method of claim 1, wherein the method operation of striking a plasma in the etch chamber while flowing the $SiCl_4$ gas includes,

generating an oxygen based plasma.

6. The method of claim 1, wherein the method operation of striking a plasma in the etch chamber while flowing the $SiCl_4$ gas includes,

maintaining a plasma density between about $1x10^9/cm^3$ and about $1x10^{12}/cm^3$.

7. The method of claim 1, wherein the method operation of striking a plasma in the etch chamber while flowing the $SiCl_4$ gas includes,

maintaining an ion energy between about 150 volts and about 400 volts.

8. The method of claim 6, wherein the method operation of maintaining a plasma density between about $1x10^9/cm^3$ and about $1x10^{12}/cm^3$ includes,

establishing a chamber pressure between about 3 milliTorr and about 15 milliTorr; and

setting a power level for a top electrode of the etch chamber between about 300 watts and about 1000 watts.

9. The method of claim 7, wherein the method operation of maintaining an ion energy between about 150 volts and about 400 volts includes,

establishing a radio frequency (RF) peak voltage for a bottom electrode between about 200 volts and 300 volts.

10. The method of claim 1, wherein the method operation of striking a plasma in the etch chamber while flowing the $SiCl_4$ gas includes,

maintaining a chamber temperature between about 20 degrees Celsius and about 70 degrees Celsius.

11. In an etch chamber a method for controlling critical dimension bias during a bilayer resist etch, comprising method operations of:

striking an oxygen based plasma in a chamber while flowing $SiCl_4$ gas into the chamber;

maintaining a plasma density between about $1x10^9/cm^3$ and about $1x10^{12}/cm^3$; and

etching each layer of the bilayer resist.

12. The method of claim 11, wherein the method operation of striking an oxygen based plasma in a chamber while flowing $SiCl_4$ gas into the chamber includes,

flowing chlorine gas into the etch chamber;

flowing hydrogen bromide (HBr) gas into the chamber; and

flowing an inert gas into the chamber.

13. The method of claim 11, wherein the method operation of striking an oxygen based plasma in a chamber while flowing $SiCl_4$ gas into the chamber includes,

flowing the $SiCl_4$ gas into the chamber between a flow rate of about 0.1 standard cubic centimeters per minute (sccm) and 6 sccm.

14. The method of claim 11, further comprising:

maintaining an ion energy between about 150 volts and about 400 volts.

15. The method of claim 14, wherein the method operation of maintaining an ion energy between about 150 volts and about 400 volts includes,

establishing a radio frequency (RF) peak voltage for a bottom electrode between about 200 volts and 300 volts.

16. The method of claim 11, wherein the method operation of maintaining a plasma density between about $1x10^9/cm^3$ and about $1x10^{12}/cm^3$ includes,

maintaining a power level associated with a top electrode between about 300 watts and about 1000 watts.

17. The method of claim 12, further comprising:

maintaining a ratio of a flow rate for oxygen gas into the chamber to a flow rate of the chlorine gas into the chamber at about 10:1.

18. The method of claim 12, wherein a flow rate of the inert gas is between about 50 sccm and about 200 sccm, a flow rate for the HBr gas is between about 50 and about 100 sccm, and a flow rate for the chlorine gas is between about 10 sccm and about 50 sccm.

19. The method of claim 11, wherein the bilayer resist includes a first layer disposed over a second layer, the first layer containing silicon.