What is claimed is:

1. A memory device comprising:

a memory cell array configured to store a valid data array, a base array and a target data array for a sparse matrix vector multiplication, the valid data array sequentially including valid elements among elements of a sparse matrix, the base array sequentially including position elements indicating position values corresponding to the valid elements, the target data array sequentially including target elements of a vector corresponding to the position values;

an information register configured to store indirect memory access information including a start address of the target data array and a unit size of the target elements; and

a prefetch circuit configured to prefetch, based on the indirect memory access information, the target elements corresponding to the position elements that are read from the memory cell array.

2. The memory device of claim 1, wherein the indirect memory access information is provided from an external memory controller to the memory device.

3. The memory device of claim 1 or claim 2, wherein the memory cell array includes a plurality of memory banks, and

wherein the valid data array, the base array and the target data array are stored in different memory banks among the plurality of memory banks.

4. The memory device of any one of claims 1 to 3, wherein the prefetch circuit includes:

an arithmetic circuit configured to calculate target addresses corresponding to the read position elements based on the read position elements, the start address of the target data array and the unit size of the target elements;

a target address register configured to store the target addresses calculated by the arithmetic circuit; and

a target data register configured to store the target elements that are read from the target addresses of the memory cell array.

5. The memory device of claim 4, wherein the arithmetic circuit calculates an i-th one of the target addresses by multiplying the unit size by B(i)-1 and adding the start address to a result of the multiplying, where B(i) indicates an i-th one of the position elements in the base array.

6. The memory device of claim 4 or claim 5, wherein the arithmetic circuit includes:

NR arithmetic units configured to provide in parallel NR target addresses based on NR of the position elements that are read simultaneously from the memory cell array where NR is a natural number greater than one.

7. The memory device of claim 6, wherein, when a total number of the position elements is NT, the NR arithmetic units provides NT target addresses by repeatedly performing address calculations NT/NR times, where NT is a natural number greater than one.

8. The memory device of any one of claims 4 to 7, wherein the target data

register is implemented with a static random access memory (SRAM).

9. The memory device of any one of claims 1 to 6, wherein the indirect memory access information further includes a start address of the base array, a unit size of the position elements, a total number of the position elements and a read number of the position elements that are read simultaneously from the memory cell array.

10. The memory device of claim 1 or claim 2, further comprising:

a calculation circuit configured to perform a processing-in-memory operation based on the sparse matrix and the vector to provide calculation result data.

11. The memory device of claim 10,

wherein the processing-in-memory operation performs a sparse matrix vector multiplication.

12. A memory device comprising:

a plurality of memory semiconductor dies stacked in a vertical direction in which memory cell arrays are formed, the memory cell arrays storing a valid data array, a base array and a target data array for a sparse matrix vector multiplication, the valid data array sequentially including valid elements among elements of a sparse matrix, the base array sequentially including position elements indicating position values corresponding to the valid elements, the target data array sequentially including target elements of a vector corresponding to the position values;

a plurality of through-silicon vias electrically connecting the plurality of memory semiconductor dies;

an information register configured to store indirect memory access information including a start address of the target data array and a unit size of the target elements; and

a prefetch circuit configured to prefetch, based on the indirect memory access information, the target elements corresponding to the position elements that are read from the memory cell array.

13. The memory device of claim 12, wherein the prefetch circuit is located in the memory semiconductor die in which the memory cell array storing the valid data array, the base array and the target data array are located.

14. The memory device of claim 12 or claim 13, further comprising:

a logic semiconductor die including a circuit for controlling access to the memory cell arrays,

wherein the prefetch circuit is formed in the logic semiconductor die.

15. The memory device of any one of claims 12 to 14, wherein the indirect memory access information is provided from an external memory controller to the memory device.

16. The memory device of any one of claims 12 to 15, wherein the prefetch circuit provides in parallel NR target addresses based on NR position elements that are read simultaneously from the memory cell array where NR is a natural number greater than one.

17. A memory device comprising:

a memory cell array configured to store a valid data array, a base array and a target

data array for a sparse matrix vector multiplication, the valid data array sequentially including valid elements among elements of a sparse matrix, the base array sequentially including position elements indicating position values corresponding to the valid elements, the target data array sequentially including target elements of a vector corresponding to the position values;

a random access memory (RAM); and

a controller configured to receive indirect memory access information including a start address of the target data array and a unit size of the target elements, from an external device,

wherein the controller performs a prefetching operation in response to receipt of the indirect memory access information, wherein the prefetching operation reads the target elements using the start address and the unit size and stores the read target elements into the RAM.

18. The memory device of claim 17, wherein the prefetching operation calculates target addresses corresponding to the read position elements based on the read position elements, the start address and the unit size and performs the reads using the calculated target addresses.

19. The memory device of claim 18, wherein the controller calculates an i-th one of the target addresses by multiplying the unit size by B(i)-1 and adding the start address to a result of the multiplying, where B(i) indicates an i-th one of the position elements in the base array.