Description

Background of the invention

The present invention relates to an FM demodulator for detecting a signal which has been frequency modulated by a digital signal and, more particularly, to an FM demodulator suitable for an integrated circuit.

An FM demodulator in an integrated circuit configuration may be implemented by a so-called direct conversion system. The system is such that a received signal is directly frequency converted to a baseband signal to allow filtering and other kinds of processing to be achieved in the baseband. Signal processing in the baseband may be accomplished by a well known method which employs differentiation and multiplication. While the differentiation and multiplication scheme is capable of demodulating even a signal which has been modulated by an analog signal, it is difficult to be implemented by an integrated circuit due to the need for an automatic gain control circuit and an analog multiplier.

An example of prior art FM demodulators of the type using the direct conversion system is disclosed in U.K. Patent Application GB 2 106 359A. The disclosed FM demodulator, as shown in Fig. 11a of the drawings, has a demodulator construction furnished with digital circuit portions and an analog circuit portion which comprises a switch, resistors, a low-pass filter and other elements. The problem encountered with such a prior art demodulator is that the analog circuit portion is not suitable for an integrated circuit implementation and minute pulse noise (spike noise) appears in an output of the demodulator due to a delay difference between two inputs of a second Exclusive-OR gate (15).

GB—A—2 032 737 proposes a radio receiver of the type applicable to radio paging systems and some navigation systems. A tone detector consisting of a bandpass filter and a rectifier detector follow a flip-flop detector so that FM tone signals are used for carrying information. GB—A—2 057 820 discloses a receiver which is implemented by frequency shift keyed (FSK) signals and with a particular modulation format. However, this circuit is based on a state transition (sequential) technique for realizing a digital logic network. EP—A—0 070 695 teaches a radio receiver in which a 90 degrees phase shifter is used to effect Hilbert conversion prior to band-limiting. EP—A—0 076 095 shows and describes a radio receiver which is elaborated to demodulate analog frequency modulated signals.

Summary of the invention

It is therefore an object of the present invention to provide an FM demodulator with reduced space requirements and reduced power consumption and feasible for an integated circuit. This object is solved with the features of the claim.

In accordance with the present invention, an FM demodulator for detecting a signal which has been frequency modulated by a digital signal is disclosed. The FM demodulator includes mixers, low-pass filters and limitters. All the circuit elements succeeding the mixers are operable in the baseband, while all the circuit elements succeeding the limitters are comprised of digital circuit elements. The FM demodulator with such a construction is suitable for an integrated circuit.

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description taken with the accompanying drawings.

Brief description of the drawings

Fig. 1 is a block diagram of an FM demodulator embodying the present invention;

Fig. 2 is a block diagram of a reference signal generator included in the FM demodulator of Fig. 1;

Fig. 3 is a circuit diagram showing the pulse generator included in the reference signal generator of Fig. 2;

Figs. 4 and 5 are timing charts representative of the operation of the FM demodulator shown in Figs. 1—3;

Fig. 6 is a block diagram showing another embodiment of the present invention;

Fig. 7 is a timing chart representative of the operation of the FM demodulator shown in Fig. 6;

Fig. 8 is a circuit diagram showing a reference signal generator shown in Fig. 6;

Fig. 9 is a block diagram showing still another embodiment of the present invention; and

Fig. 10 is a timing chart demonstrating the operation of the FM demodulator shown in Fig. 9.

Description of the preferred embodiments

While the FM demodulator of the present invention is susceptible of numerous physical embodiments, depending upon the environment and requirements of use, substantial numbers of the herein shown and described embodiments have been made, tested and used, and all have performed in an eminently satisfactory manner.

Referring to Fig. 1 of the drawings, an FM demodulator embodying the present invention is shown and generally designated by the reference numeral 10. A received signal which has undergone frequency modulation by a mark or space digital signal is applied to an input terminal 12 and routed therefrom to mixers 14 and 16. A local oscillator 18 produces an output whose frequency is substantially equal to the center frequency of the input signal. The oscillator output is applied on one hand to the mixer 14 and on the other hand to the mixer 16 via a 90° phase shifter 20 so that the mixers 14 and 16, using the local oscillation signals which are different in phase by 90°, frequency convert the received signal to the baseband signal. The mixer 14 is connected to a low-pass filter (LPF) 22 and the mixer 16 to a low-pass filter (LPF) 24. Each of the LPFs 22 and 24 functions to pick up only a baseband signal in a desired channel and to band-limit the noise. The

baseband signals output from the low-pass filters 22 and 24 respectively are applied to limitters 26 and 28 which then produce digital signals I and Q, respectively. Since the phase difference between the modulated signal routed from the input terminal 12 to the mixer 16 and the output of the phase shifter 20 and the phase difference between the modulated signal routed to the mixer 14 and the output of the local oscillator 18 differs by 90°, the signals I and Q are also different in phase by 90° from each other. Exemplary waveforms of the signals I and Q are shown in Fig. 4, in which the solid lines show a case wherein the modulation signal is a mark and the phantom lines a case wherein the modulation signal is a space.

The signals I and Q are coupled to an Exclusive-OR (Ex-OR) gate 30 which produces a signal IQ as shown in Fig. 4. At the same time, the signals I and Q are applied to a reference signal generator 32. As will be described later in detail, the reference signal generator 32 is constructed to generate a reference signal Z which shares the same period with the signals I and Q and, whether the modulation signal is a mark or a space, does not change its phase relative to the signal I or Q. The signal Z is routed to another Ex-OR gate 34 together with the signal IQ. As shown in Fig. 4, an output signal X of the Ex-OR 34, except for its minute pulse portions, becomes logical "1 (solid line)" or "0 (phantom line)" level depending upon the modulation signal which is either a mark or a space, whereby frequency detection is accomplished. The minute pulse portion originates from some time difference in transition point between the two signals applied to the Ex-OR gate 34.

In accordance with the present invention, a D-type flip-flop 38 samples and holds the signal X using an output signal DZ of a pulse generator 36 as a clock signal, for the purpose of removing the above-discussed minute pulse portions. The signal DZ is acceptable only if not generated while the signal X appears in minute pulse portions, that is, only if generated either before or after minute pulse portions of the signal X with respect to time, and may be generated by cascading delay circuits by way of example. The input signal to the delay and pulse generator 36 does not have to be the reference signal Z and may even be the signal IQ. This will readily be understood from the fact that a pulse generator, which will be described, is constructed to generate a pulse at a transition point of a signal, and that the transitions of the signals IQ and Z correspond in one-to-one relation to each other.

Referring to Fig. 2, a detailed construction of the reference signal generator 32 in accordance with the illustrative embodiment is shown. The signals I and Q respectively are applied to input terminals 320 and 322 and, therefrom, to pulse generators 324 and 326. As shown in Fig. 5, the pulse generators 324 and 326 produce pulse signals DI and DQ, respectively, each at transition points of the input signal I or Q. A set-reset flip-flop 328 is set by the pulse signal DQ and reset by the signal DI to produce the reference signal Z at an output terminal 330 thereof. The reference signal Z is dependent upon the transition time of the signals I and Q only and not upon whether the modulation signal is a mark or a space.

Each of the pulse generators 324 and 326 may be constructed as shown in Fig. 3 by way of example. In Fig. 3, the signal applied to an input terminal 332 is coupled to an Ex-OR gate 336 directly on one hand and via a delay circuit 334 on the other hand. Appearing at an output terminal 338, therefore, are pulses which are timed to transitions of the input signal.

In accordance with the embodiment described above, the phase difference between the signals I and Q is not limited to 90° which is most preferable and is free to choose insofar as it is not zero. This will easily be seen by, for example, drawing such waveforms as those shown in Fig. 4.

The phase difference between the signals I and Q may be provided by developing a phase difference in the modulated signal which is input to the two mixers 14 and 16, instead of developing it in the local oscillation signal as shown and described.

Furthermore, the signals Q and I coupled to the set and reset terminals of the flip-flop 328 may be replaced with each other. Any of such combinations of the signals Q and I is successful to provide a detected signal with marks and spaces appearing correctly or changed for each other. In the latter case, a circuit for inverting the data will be added to the illustrated arrangement.

Referring to Fig. 6, an FM demodulator 40 in accordance with another embodiment of the present invention is shown. The frequency-modulated signal is applied to an input terminal 42 of the FM demodulator 40. A local oscillator 44 generates a signal whose frequency is substantially equal to the center frequency of the input modulated signal. The output of the local oscillator 44 is applied to a phase splitter 46 to be thereby provided with phase differences of 0°, 45°, 90° and 135°. The four outputs of the phase splitter 46 respectively are fed to four mixers 48, 50, 52 and 54 as local oscillation signals, each of the mixers frequency converting the input modulated signal to the baseband signal on the basis of the associated local oscillation signal. The outputs of the mixers 48, 50, 52 and 54 respectively are passed through low-pass filters 56, 58, 60 and 62 and then through limitters 64, 66, 68 and 70 to become signals I_1, Q_1, I_2 and Q_2. These signals may have waveforms as shown in Fig. 7 by way of example. In Fig. 7, solid lines are associated with a mark and phantom lines with a space. The signals I_1, Q_1, I_2 and Q_2 are applied to an Ex-OR gate 72 which then produces an output signal IQ as shown in Fig. 7. The signal IQ is coupled to another Ex-OR gate 76 together with a reference signal Z which is generated by a reference signal generator 74. As shown in Fig. 7, an output signal X of the Ex-OR gate 76 becomes logical "1 (solid line)" level or "0 (phantom line)" level depending upon the modulation signal which is the mark or

space except for minute pulse portions. A delay and pulse generator 78 and a D-type flip-flop 80 function in the same manner as those of the first embodiment.

The reference signal generator 74 in the illustrative embodiment may be implemented by the circuitry shown in Fig. 8. The operation of the circuitry of Fig. 8 will not need detailed description. Let it suffice to say that Ex-OR gates 740 and 742 and a delay circuit 744 cooperate to generate pulses at the leading edges and trailing edges of the signals I_2 and Q_2 to thereby set a set-reset flip-flop 746, while Ex-OR gates 748 and 750 and a delay circuit 752 in cooperation generate pulses at the leading edges and trailing edges of the signals I_1 and Q_1 to thereby reset the flip-flop 746, the output Z appearing at an output terminal 754. Although more complicated in construction than the first embodiment, the second embodiment will prove particularly effective where the phase transition of the modulated signal is relatively insignificant, that is, where the modulation index is smaller.

Referring to Fig. 9, still another embodiment of the present invention is shown. An FM demodulator, generally 90, is common to the FM demodulator 40 concerning the constructions and operations of the mixers 48, 50, 52 and 54, low-pass filters 56, 58, 60 and 62, limitters 64, 66, 68 and 70, phase splitter 46, and oscillator 44. In accordance with this particular embodiment, the digital outputs I_1, Q_1, I_2 and Q_2 have individual phase differences which correspond to those provided by the phase splitter 46 as shown in Fig. 10, in which solid lines show a case wherein the modulation signal is the mark and phantom lines a case wherein it is the space. The signals I_1 and Q_1 are applied to an Ex-OR gate 92 and the signals I_2 and Q_2 to another Ex-OR gate 94 whereby signals I_1Q_1 and I_2Q_2 are produced as shown in Fig. 10. At the same time, the signals I_1 and Q_1 are routed to the reference signal generator 32, which is constructed in the same way as in Fig. 2, to provide the reference signal Z. The reference signal Z and the signal I_1Q_1 are applied to an Ex-OR gate 96 which then produces an output signal X. As shown in Fig. 10, the signal X becomes logical "1 (solid line)" level or "0 (phantom line)" level depending upon the modulation signal which is the mark or the space, except for minute pulse portions. In this embodiment, the signal I_2Q_2 is fed to the pulse generator 324 (326) which has the construction shown in Fig. 3, so as to produce a pulse signal DI_2Q_2, while a D-type flip-flop 98 samples the signal X clocked by the pulse signal DI_2Q_2. As shown in Fig. 10, the pulses DI_2Q_2 are each developed in between the successive minute pulse portions of the signal X and, therefore, free from the influence of the minute pulse portions.

In the second and third embodiments described above, it should be noted that the 45° of phase difference between the signals I_1, Q_1, I_2 and Q_2 is not limitative and any other suitable angle other than zero may be selected, as will readily be seen by drawing such waveforms as those of Fig. 10.

Further, the number of the base band signals is not limited to four and may be increased to $4\times N$ (positive integer) without effecting the operation, as can also be confirmed. For example, assume eight baseband signals which have relative phases of 0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135° and 157.5°. Then, assuming that the signals with the phases 0°, 45°, 90° and 135° belong to a first group and the others to a second group, transition times of the signals in the second group each intervene between those of the signals in the first group. Further, assuming that the signals with the phases of 0° and 90° in the second group constitute a third group and those with the phases 45° and 135°, a fourth group, a reference signal can be generated by a set-reset circuit which is reset by transition points of the signals in the third signal group. When the reference signal is applied to an Ex-OR gate together with a signal which has been provided by applying all the signals in the first group to an Ex-OR, the signal X as shown in Fig. 10 will be produced.

Where the signals in the second group are coupled to an Ex-OR gate and, then, to such a pulse generator as one shown in Fig. 3, the resulting sampling pulses each appear at a time intermediate between successive transition points of the first signal group, that is, avoiding the minute pulse portions of the signal X. The signal X can therefore be sampled by a sampling circuit using the sampling pulses.

The gist is that the signals to be grouped are arranged in the order of the phase. However, where the phase difference exceeds 180°, the signals have to be arranged in the modulo 180° order. Again, such will readily be understood by drawing waveforms.

In summary, it will be seen that the present invention provides an FM demodulator which is attainable as an integrated circuit with ease since all the circuit elements succeeding mixers are operable in the baseband and those succeeding limitters are implemented by digital circuit elements. The arrangement succeeding the baseband circuit may be implemented by once digitizing the signals and, then, effecting signal processing in accordance with the present invention by means of a microprocessor or the like.

Claim

An FM demodulator comprising:

frequency conversion means (14, 16, 48, 50, 52, 54) to which is applied a signal being frequency-modulated by a digital signal for providing two baseband signals which are different in phase from each other in response to a signal having a frequency which is substantially equal to a center frequency of the modulated signal;

limitter means (26, 28; 64, 66, 68, 70) for digitizing the two baseband signals to provide two digital signals (I, Q) of two logical levels;

a first Exclusive-OR gate (30; 72; 92, 94) for providing Exclusive-OR of the two digital signals to produce a first gate signal (IQ);

space except for minute pulse portions. A delay and pulse generator 78 and a D-type flip-flop 80 function in the same manner as those of the first embodiment.

The reference signal generator 74 in the illustrative embodiment may be implemented by the circuitry shown in Fig. 8. The operation of the circuitry of Fig. 8 will not need detailed description. Let it suffice to say that Ex-OR gates 740 and 742 and a delay circuit 744 cooperate to generate pulses at the leading edges and trailing edges of the signals I_2 and Q_2 to thereby set a set-reset flip-flop 746, while Ex-OR gates 748 and 750 and a delay circuit 752 in cooperation generate pulses at the leading edges and trailing edges of the signals I_1 and Q_1 to thereby reset the flip-flop 746, the output Z appearing at an output terminal 754. Although more complicated in construction than the first embodiment, the second embodiment will prove particularly effective where the phase transition of the modulated signal is relatively insignificant, that is, where the modulation index is smaller.

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In the second and third embodiments described above, it should be noted that the 45° of phase difference between the signals I_1, Q_1, I_2 and Q_2 is not limitative and any other suitable angle other than zero may be selected, as will readily be seen by drawing such waveforms as those of Fig. 10.

Further, the number of the base band signals is not limited to four and may be increased to $4\times N$ (positive integer) without effecting the operation, as can also be confirmed. For example, assume eight baseband signals which have relative phases of 0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135° and 157.5°. Then, assuming that the signals with the phases 0°, 45°, 90° and 135° belong to a first group and the others to a second group, transition times of the signals in the second group each intervene between those of the signals in the first group. Further, assuming that the signals with the phases of 0° and 90° in the second group constitute a third group and those with the phases 45° and 135°, a fourth group, a reference signal can be generated by a set-reset circuit which is reset by transition points of the signals in the third signal group. When the reference signal is applied to an Ex-OR gate together with a signal which has been provided by applying all the signals in the first group to an Ex-OR, the signal X as shown in Fig. 10 will be produced.

Where the signals in the second group are coupled to an Ex-OR gate and, then, to such a pulse generator as one shown in Fig. 3, the resulting sampling pulses each appear at a time intermediate between successive transition points of the first signal group, that is, avoiding the minute pulse portions of the signal X. The signal X can therefore be sampled by a sampling circuit using the sampling pulses.

The gist is that the signals to be grouped are arranged in the order of the phase. However, where the phase difference exceeds 180°, the signals have to be arranged in the modulo 180° order. Again, such will readily be understood by drawing waveforms.

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Claim

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limitter means (26, 28; 64, 66, 68, 70) for digitizing the two baseband signals to provide two digital signals (I, Q) of two logical levels;

a first Exclusive-OR gate (30; 72; 92, 94) for providing Exclusive-OR of the two digital signals to produce a first gate signal (IQ);

reference signal generator means (32; 74) applied with the two digital signals (I, Q) for generating a reference signal (Z) by selecting one of logical "1" and "0" levels every time a state of one of the two digital signals is changed and selecting the other logical level every time a state of the other digital signal is changed;

a second Exclusive-OR gate (34; 76; 96) applied with the reference signal (Z) and the first gate signal to produce a second gate signal (X);

pulse generator means (36; 78, 324) applied with one of the second gate signal and the reference signal as an input signal for generating a pulse signal in response to a state transition of the input signal and before or after a time of the state transition; and

a D-type flip-flop (38; 80; 98) applied with the pulse signal as a clock pulse input and the second gate signal as a signal input, an output of the D-type flip-flop being delivered as a detected output signal.

Patentanspruch

Demodulator für frequenzmodulierte Signale mit

einem Frequenzwandler (14, 16; 48, 50, 52, 54), dem ein Signal zugeführt wird, das durch ein Digitalsignal moduliert ist, um zwei Basisband-Signale, die voneinander phasenverschieden sind, in Abhängigkeit von einem Signal zu erzeugen, dessen Frequenz im wesentlichen gleich einer Mittelfrequenz des modulierten Signals ist;

einem Begrenzer (26, 28; 64, 66, 68, 70) zum Digitalisieren der zwei Basisband-Signale und Erzeugen zweier Digitalsignale (I, Q) mit zwei Logikpegeln;

einer ersten Exklusiv-ODER-Torschaltung (30; 72; 92, 94) zum Bilden des Exklusiv-ODER der zwei Digitalsignale und Erzeugen eines ersten Torsignals (IQ);

einem Bezugssignalgenerator (32; 74) dem die zwei Digitalsignale (I, Q, zugeführt werden, um ein Bezugssignal (Z) zu Erzeugen zum Auswählen eines der Logikpegel "1" und "0" zu jedem Zeitpunkt, wenn ein Zustand eines der beiden Digitalsignale geändert wird, und Auwählen des anderen Logikpegels zu jedem Zeitpunkt, wenn ein Zustand des anderen Digitalsignals geändert wird;

einer zweiten Exklusiv-ODER-Torschaltung (34, 76; 96), der das Bezugssignal (Z) und das erste Torsignal zugeführt wird, um ein zweites Torsignal (X) zu erzeugen;

einem Impulsgenerator (36; 78; 324), dem entweder das zweite Torsignal oder das Bezugssignal als Eingangssignal zugeführt wird, um ein Impulssignal in Abhängigkeit von einem Zustandsübergang des Eingangssignals und vor oder nach einem Zeitpunkt des Zustandsübergangs zu erzeugen; und mit

einem D-Flip-Flop (38; 80; 98), dem das Impulssignal als Taktimpulseingang und das zweite Torsignal als Signaleingang zugeführt wird, wobei ein Ausgang des D-Flip-Flop als ein detektiertes Ausgangssignal abgegeben wird.

Revendication

Démodulateur MF comprenant:

un moyen de conversion de fréquence (14, 16; 48, 50, 52, 54) auquel est appliqué un signal modulé par un signal numérique afin de fournir deux signaux de bande de base qui ont des phases différentes l'une de l'autre en réponse à un signal présentant une fréquence qui est sensiblement égale à la fréquence centrale du signal modulé;

un moyen de limiteur (26, 28; 64, 66, 68, 70) pour numériser les deux signaux de bande de base afin de fournir deux signaux numériques (I, Q) de deux niveaux logiques;

une première porte OU Exclusif (30; 72; 92, 94) pour fournir une action OU Exclusif des deux signaux numériques afin de produire un premier signal de porte (IQ);

un moyen de générateur de signal de référence (32, 74) auquel sont appliqués les deux signaux numériques (I, Q) pour produire un signal de référence (Z) en choisissant l'un des niveaux logiques "1" et "0" chaque fois que l'état un des deux signaux numériques est changé et en choisissant l'autre niveau logique chaque fois que l'état de l'autre signal numérique est modifié;

une seconde porte OU Exclusif (34; 76; 96) à laquelle sont appliqués le signal de référence (Z) et le premier signal de porte afin de produire un second signal de porte (X);

un moyen de générateur d'impulsions (36; 78; 324) auquel est appliqué le second signal de porte ou le signal de référence comme signal d'entrée afin de produire un signal impulsionnel en réponse à une transition d'état du signal d'entrée et avant ou après l'instant de la transition d'état; et

une bascule du type D (38; 80; 98) à laquelle sont appliqués le signal impulsionnel comme impulsion d'horloge d'entrée et le second signal de porte comme signal d'entrée, une sortie de la bascule du type D étant délivrée comme signal de sortie détecté.

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