What is claimed is:

1. A stacked memory device, comprising:

a logic semiconductor die;

a plurality of memory semiconductor dies stacked with the logic semiconductor die, wherein each of the memory semiconductor dies includes a memory integrated circuit and more than one of the memory semiconductor dies are calculation semiconductor dies each including a calculation unit; and

through-silicon vias electrically connecting the logic semiconductor die and the plurality of memory semiconductor dies;

wherein each of the calculation units is configured to perform calculations based on broadcast data and internal data and to generate calculation result data, wherein the broadcast data is commonly provided to the calculation semiconductor dies through the through-silicon vias, and the internal data is respectively read from the memory integrated circuits of the calculation semiconductor dies.

2. The stacked memory device of claim 1, wherein each of the memory semiconductor dies includes a plurality of memory banks and the calculation units are disposed in the memory banks included in the calculation semiconductor dies.

3. The stacked memory device of claim 2, wherein the calculation units included in the memory banks of the calculation semiconductor dies commonly receive the broadcast data and perform the calculations based on the broadcast data simultaneously.

4. The stacked memory device of claim 2 or claim 3, wherein each of the memory banks includes a plurality of data blocks and each of the calculation units is assigned with respect to a predetermined number of the data blocks.

5. The stacked memory device of any one of claims 1 to 4, wherein each of the calculation units includes first input terminals for receiving the internal data and second input terminals for receiving the broadcast data, the first input terminals are connected to output terminals of an input-output sense amplifier that amplifies signals on global input-output lines and the second input terminals are connected to input terminals of an input-output driver that drives the global input-output lines.

6. The stacked memory device of any one of claims 1 to 5, wherein at least one of the memory semiconductor dies is an input-output semiconductor die that does not include the calculation units.

7. The stacked memory device of claim 6, wherein the broadcast data are transferred directly from the input-output semiconductor die to the calculation semiconductor dies without passing through the logic semiconductor die.

8. The stacked memory device of claim 6 or claim 7, wherein the input-output semiconductor die simultaneously drives data buses with the broadcast data and each of the calculation semiconductor dies receives the broadcast data through a corresponding one of the data buses.

9. The stacked memory device of claim 6, wherein the input-output semiconductor die drives a data bus corresponding to the input-output semiconductor die with the broadcast data and each of the calculation semiconductor dies receives the broadcast data through the data bus corresponding to the input-output semiconductor die.

10. The stacked memory device of any one of claims 6 to 9, wherein the calculation result data are transferred from the calculation semiconductor dies to the logic semiconductor die, and then, transferred from the logic semiconductor die to the input-output semiconductor die.

11. The stacked memory device of claim 10, wherein the calculation result data are simultaneously transferred from the calculation semiconductor dies to the logic semiconductor die through data buses respectively corresponding to the calculation semiconductor dies, and the calculation result data are sequentially transferred from the logic semiconductor die to the input-output semiconductor die by a time-division scheme through the data bus corresponding to the input-output semiconductor die.

12. The stacked memory device of claim 6, wherein the calculation result data are transferred directly from the calculation semiconductor dies to the input-output semiconductor die without passing through the logic semiconductor die.

13. The stacked memory device of claim 12, wherein each of the calculation semiconductor dies drives a corresponding data bus with the calculation result data and the input-output semiconductor die receives the calculation result data sequentially through the

data buses corresponding to the calculation semiconductor dies.

14. The stacked memory device of claim 12, wherein the calculation semiconductor dies sequentially drive a data bus corresponding to the input-output semiconductor die with the calculation result data, and the input-output semiconductor die sequentially receives the calculation result data through the data bus corresponding to the input-output semiconductor die.

15. The stacked memory device of any one of claims 1 to 5, wherein all of the memory semiconductor dies are the calculation semiconductor dies that include the calculation units.

16. The stacked memory device of any one of claims 2 to 5, wherein each of the calculation semiconductor dies further includes a plurality of bank adders, and each of the bank adders sums outputs of the calculation units in each of the memory banks to generate bank result signals.

17. The stacked memory device of any one of claims 1 to 5, wherein each of the calculation units includes:

a multiplication circuit configured to multiply the broadcast data and the internal data; and

an accumulation circuit configured to accumulate outputs of the multiplication circuit to provide the calculation result data.

18. The stacked memory device of any of claims 1 to 17, wherein the logic semiconductor die further includes a data transform logic configured to process data provided from the memory semiconductor dies or data provided from an external device.

19. A memory system, comprising:

a base substrate:

at least one logic semiconductor die stacked on the base substrate;

a plurality of memory semiconductor dies stacked on the base substrate or on the logic semiconductor die; and

a plurality of calculation units formed in more than one calculation semiconductor dies among the plurality of memory semiconductor dies, wherein each of the calculation units is configured to perform calculations based on broadcast data and internal data and to generate calculation result data, wherein the broadcast data is commonly provided to the calculation semiconductor dies, and the internal data is respectively read from memory integrated circuits of the calculation semiconductor dies.

20. A method of operating a stacked memory device, the stacked memory device including a calculation unit in each of a plurality of calculation semiconductor dies stacked in a vertical direction, the method comprising:

providing broadcast data, in common, to each of the calculation units through through-silicon vias electrically connecting the calculation semiconductor dies;

providing internal data respectively read from memory integrated circuits of the calculation semiconductor dies to each of calculation units; and

performing a plurality of calculations based on the broadcast data and the internal

data simultaneously using the calculation units.