

DEFLECTION CIRCUIT WITH SERVICE MODE OPERATION

This invention relates to a deflection circuit with service mode operation and is divided from our application No. 8719262 ("the parent application").

5 To manually adjust the color temperature in a television receiver or other video display apparatus, various circuits in the television receiver are disabled including the vertical deflection circuit. The vertical deflection circuit is disabled in order to collapse the raster into a
10 single (horizontal) line. A service switch may be used to ground or otherwise apply a disabling potential at a point in the vertical deflection circuit that prevents the generation of vertical deflection current.

When the vertical deflection circuit includes a
15 push-pull output stage, the vertical deflection circuit may be disabled in such a manner as to disable the AC vertical sawtooth generator or to bias the push-pull output stage into developing only a DC voltage at its output terminal. The DC blocking capacitor coupled to the vertical
20 deflection winding will remain charged during service mode of operation. The voltage level to which the DC blocking capacitor is charged during service mode operation may undesirably be greater than the normal DC operating voltage level.

25 In accordance with the present invention, a deflection circuit with a service mode arrangement comprises a deflection winding, and a deflection amplifier having an output terminal coupled to the deflection winding and being responsive to a deflection rate drive
30 signal for generating a deflection rate deflection current in the deflection winding. An error amplifier having an input terminal coupled to said output terminal, has an output terminal, at which there is developed an error voltage, coupled to an input terminal of the deflection
35 amplifier to form a negative feedback loop for stabilizing a DC voltage level at the output terminal of the

deflection amplifier. Service mode means coupled to the output terminal of the error amplifier applies thereto during service mode operation a DC bias voltage that overrides the error voltage for disabling the generation
5 of the deflection rate deflection current.

The accompanying drawing illustrates a vertical deflection circuit with service mode operation, embodying the present invention and also that of the parent application.

10 In the illustrated vertical deflection circuit 20 for a television receiver or other video display apparatus, a vertical deflection winding L_V is coupled to a vertical amplifier output stage 21 at an output terminal A. A current sampling resistor R8 is coupled to deflection
15 winding L_V at a terminal C, and a DC blocking and S-shaping capacitor C_V is coupled to resistor R8 at a terminal D.

Vertical output stage 21 includes a top amplifier transistor Q4 coupled to a +24V DC supply via a diode D2 and a bottom amplifier transistor Q3 coupled to a ground
20 reference potential point. A driver stage 22 is coupled to output stage 21 for driving the output stage at a vertical rate in a sawtooth manner to generate a sawtooth vertical deflection current i_V in vertical deflection winding L_V .

25 Driver stage 22 includes an inverting amplifier, driver transistor Q2, and a current source 23 coupled to the collector of the transistor. Driver transistor Q2 drives top output transistor Q4 via a non-inverting buffer transistor Q5 and drives bottom output transistor Q3 via
30 an inverting stage U1 and a non-inverting buffer transistor Q6. The driver and output stages may be incorporated into an integrated circuit, IC 1, such as the LA7831, manufactured by Sanyo Corporation.

To generate a vertical sawtooth current i_V in
35 vertical deflection winding L_V , a vertical ramp generator 26 generates a downwardly going vertical ramp voltage 27 that is AC coupled by a capacitor C2 to the base of an

error amplifier transistor Q1. Error amplifier transistor Q1 inverts vertical ramp voltage 27 to develop a vertical input voltage 28 across a collector load resistor R1 of transistor Q1. Input voltage 28 is applied to an input terminal B of driver stage 22 that is coupled to the base of inverting amplifier transistor Q2 via a resistor R2.

Vertical input voltage 28 progressively increases the conduction of driver transistor Q2 during the vertical trace interval, progressively shunting more of current I₁, developed by current source 23, away from top output amplifier portion Q5 and Q4. During the first half of trace, output transistor Q4 is conducting, to couple the +24V supply to vertical deflection winding L_V via diode D2. A decreasing vertical deflection current i_V flows in deflection winding L_V and charges DC blocking capacitor C_V from the +24V supply via transistor Q4.

During the second half of vertical trace, driver transistor Q2 has been made sufficiently conductive by input voltage 28 to turn off top output transistor Q4 and turn on bottom output transistor Q3. DC blocking capacitor C_V discharges to ground via vertical deflection winding L_V and transistor Q3, thereby generating the negative sawtooth portion of vertical deflection current i_V.

To initiate the vertical retrace interval, input voltage 28 turns off driver transistor Q2, thereby turning off bottom output transistor Q3 and turning on top output transistor Q4. Conventional vertical retrace circuitry, not illustrated in the FIGURE, provides for the retrace of vertical deflection current i_V.

The operation of output stage 21 in response to vertical input voltage 28, develops a vertical output voltage 29 at output terminal A that is applied to vertical deflection winding L_V. The DC level, V₀, established at output terminal A, also establishes the same DC level at terminals C and D. Vertical deflection current i_V generates an AC sawtooth voltage between terminals C and D, across sampling resistor R8, and generates a parabolic component 30 to the voltage V_D developed across DC blocking capacitor C_V.

A DC negative feedback loop from output terminal A to input terminal B stabilizes the DC operating voltage level at terminal A. The voltage at terminal A is coupled via terminal C to the emitter of error amplifier transistor Q1 to establish the DC voltage of the emitter at voltage level V_0 . Voltage level V_0 is compared with a reference voltage level V_r that is developed at the base of transistor Q1 by voltage dividing resistors R9 and R10. The level of input voltage 28 is controlled by the conduction of transistor Q1 for stabilizing the DC voltage level V_0 at an operating level that is approximately $1V_{be}$ above reference voltage level V_r .

AC negative feedback for scan linearization is provided by coupling the AC sawtooth voltage developed across sampling resistor R8 to the emitter of error transistor Q1 via a voltage dividing network comprising potentiometer R12 and resistors R14 and R15. The AC sawtooth voltage at the emitter of error transistor Q1 is compared against reference ramp voltage 27 that is AC coupled to the base of the transistor Q1 in order to develop the AC component of input voltage 28. Deflection current amplitude is adjusted by adjusting the wiper arm of potentiometer R12.

Ramp generator 26, that develops AC reference ramp voltage 27, comprises an RC integrating network, capacitor C1 and resistor R11, and a reset switch, transistor Q7, coupled across capacitor C1. Voltage V_D developed across DC blocking capacitor C_v is applied to the integrating network of capacitor C1 and resistor R11 via a resistor R13. The DC component of voltage V_D is integrated by capacitor C1 to generate a downwardly-going ramp of voltage across resistor R11. The AC, parabolic component of voltage V_D is integrated by capacitor C1 to provide S-shaping of the ramp voltage across resistor R11.

To initiate vertical retrace, ramp capacitor C1 is discharged by making reset transistor Q7 conductive. A vertical reset pulse 36, generated by vertical synchronization circuitry not illustrated in the FIGURE, is

applied to the base of a transistor Q8, making the transistor nonconductive during the short reset pulse interval. The collector of transistor Q8 is coupled to a +8V supply by a resistor R16 and is coupled to ground by a resistor R17. The junction of the two resistors and the collector of transistor Q8 is AC coupled to the base of reset transistor Q7 via a capacitor C3 and a resistor R18. Negative going reset pulse 36 is inverted by transistor Q8 and applied to the base of transistor Q7, to turn transistor Q7 on and discharge capacitor C1. The sharp increase in ramp voltage 27 when capacitor C1 is discharged is coupled to the base of error amplifier transistor Q1 and turns the transistor off to initiate the vertical retrace interval.

A resistor R6 coupled between the collector and base of reset transistor Q7 discharges capacitor C3 to remove charge accumulated on the capacitor during the cutoff interval of transistor Q8. A resistor R5 is coupled between output terminal A and the junction of capacitor C1 and resistor R11 to introduce a compensating current that compensates for the slight exponential waveshape to the ramp current developed in resistor R11. A capacitor C5 in series with a resistor R19 across deflection winding L_V damps deflection winding resonances.

Resistor R13 provides current limiting under transient picture tube arcing conditions should the ground reference potential point for voltage V_D differ greatly from other ground reference potential points, such as for the base or emitter of error amplifier transistor Q1. A parallel network of a resistor R7 and a capacitor C4 is coupled between output terminal A and the emitter of error amplifier transistor Q1 to compensate for horizontal rate pickup by vertical deflection winding L_V . A capacitor C6 in series with a resistor R20 is coupled between input terminal B and ground to roll off the gain at higher frequencies to prevent deflection circuit high frequency oscillation.

During service mode operation of the television receiver, when, for example, color temperature is to be manually adjusted, it may be desirable to provide for vertical collapse of the raster by disabling vertical deflection circuit 20. In accordance with a feature of the invention, a service mode switching circuit 50 disables the generation of vertical deflection current in the service mode of operation. Service mode switching circuit 50 includes a current source 24 coupled to a +5V supply, a service mode switching transistor Q9 having its collector coupled to current source 24 and its emitter coupled to ground, and a diode D1, having its cathode coupled to vertical input terminal B and its anode coupled to the junction of current source 24 and the collector of transistor Q9 via a resistor R4.

During the normal mode of television receiver operation, a mode-switching signal 25, that may be conventionally generated, is in the high state, maintaining transistor Q9 in saturated conduction. Current I2 of current source 24 is shunted to ground. The near-ground potential at the collector of transistor Q9 provides reverse biasing of diode D1, thereby disconnecting service mode switching circuit 50 from vertical input terminal B.

To assert the service mode of television receiver operation, mode-switching signal 25 is switched to the low state to cutoff conduction in transistor Q9. With transistor Q9 cutoff, its collector voltage increases sufficiently to forward bias diode D1 and provide a path for current I2 to flow to input terminal B. Current I2 flows in resistor R1 and to the base of driver transistor Q2 to bias the transistor into continuous, saturated conduction.

The continuous, saturated conduction of driver transistor Q2 shunts current I1 from the top portion of output stage 21, thereby cutting off conduction in output transistor Q4. At the same time, the saturated conduction of driver transistor Q2 turns on bottom output transistor

arrangement has several advantages over other types of switching arrangements which, for example, attempt to ground vertical input terminal B through a diode in order to shunt base current away from driver transistor Q2 and
5 bring the transistor into cutoff.

Because the emitter of driver transistor Q2 is grounded via emitter resistor R3, a relatively small bias or offset voltage at the base will bring transistor Q2 out of cutoff. Approximately 0.7V is needed to offset the
10 forward base-emitter junction voltage of transistor Q2, and approximately 0.2V of additional offset voltage is needed to take into account the voltage drop across resistor R3 produced by collector-to-emitter current flow in transistor Q2. Thus, for the values illustrated in the FIGURE, the
15 voltage at the base required to bring transistor Q2 out of cutoff is near 0.9V. A service switching arrangement, that attempts to disable vertical deflection circuit 20 by shunting base current to ground via a diode coupled in parallel with the base-emitter junction of transistor Q2,
20 may, therefore, have difficulty in maintaining the voltage at terminal B below the cutoff biasing voltage level of the transistor.

Q3 and maintains this transistor in continuous, saturated conduction.

With transistor Q3 in continuous, saturated conduction during service mode of operation, DC blocking capacitor C_V is discharged to ground via this transistor. With transistor Q4 in cutoff, the +24V supply is disconnected from terminal A and from vertical deflection winding L_V , preventing the recharging of capacitor C_V . By making transistor Q3 conductive and transistor Q4 cutoff during service mode operation, instead of making transistor Q4 conductive and transistor Q3 cutoff, capacitor C_V is discharged to zero volts instead of being charged to the +24V supply level. This arrangement advantageously avoids stressing capacitor C_V during service mode operation by a voltage in excess of the normal DC operating voltage level V_0 .

To reliably maintain the television receiver in the service mode of operation, the amplitude of biasing current I2, provided by service mode switching circuit 50, is sufficiently large to develop a base biasing voltage across resistor R1 that maintains driver transistor Q2 in saturated conduction. By coupling current I2 to the output of error amplifier transistor Q1, the DC negative feedback loop is bypassed. Thus, when the DC negative feedback loop attempts to raise the DC voltage level at terminal A, in an attempt to maintain a stabilized operating voltage level V_0 during service mode operation, error amplifier transistor Q1 becomes cutoff. With error amplifier transistor Q1 cutoff, the DC negative feedback loop becomes disconnected from input terminal B and will not attempt to adversely counteract the operation of service mode switching circuit 50.

The switching arrangement of transistor Q9 and diode D1 is advantageously designed to raise the voltage level at vertical input terminal B so as to bias driver transistor Q2 into continuous, saturated conduction. By this means, vertical deflection circuit 20 is disabled during service mode operation. This type of switching

CLAIMS:

1. A deflection circuit with a service mode arrangement, comprising:

a deflection winding;

a deflection amplifier having an output terminal coupled to said deflection winding and being responsive to a deflection rate drive signal for generating a deflection rate deflection current in said deflection winding;

an error amplifier having an input terminal coupled to said output terminal and having an output terminal at which there is developed an error voltage, said output terminal being coupled to an input terminal of said deflection amplifier to form a negative feedback loop for stabilizing a DC voltage level at the output terminal of said deflection amplifier; and

service mode means coupled to the output terminal of said error amplifier for applying thereto during service mode operation a DC bias voltage that overrides said error voltage for disabling the generation of said deflection rate deflection current.

2. A deflection circuit according to Claim 1 wherein said DC bias voltage changes the DC voltage level at the output terminal of said deflection amplifier so as to cutoff said error amplifier.

3. A deflection circuit according to Claim 2 including a deflection rate ramp signal generator and means for generating a deflection rate sampling signal representative of said deflection current, said ramp and sampling signals being applied as inputs to said error amplifier to form an AC negative feedback loop that develops said deflection rate drive signal.

4. A deflection circuit substantially as hereinbefore described with reference to the accompanying drawings.

