Description

The invention relates to a fabrication technique for constructing high performance circuit boards, and more particularly to a modularized process for assembling printed circuit boards having a triplate geometry from sub-assemblies.

High density printed circuit boards are generally constructed with several electrically conductive layers separated by dielectric layers. Some of the conductive layers are used to supply power and ground voltages. The remaining conductive layers are patterned for electrical signal interconnections among integrated circuit chips. Layer-to-layer interconnections are achieved by means of through-holes plated with electrically conductive material. In high density printed circuit boards it has been normal practice to provide interconnections between adjacent conducting layers, which interconnections are commonly known as "vias".

In US-A-3 740 678 a triplate circuit board construction is shown in which X-Y signal planes form a repeating basic core structure in a multi-laminated, high density circuit board.

Such a circuit board construction has been useful in transmitting high frequency signals, and relies upon alternating dielectric mediums to achieve its many benefits.

One of the dielectric sheets comprises an epoxy glass having a relatively high dielectric constant.

Such a material is useful in providing structural stability to the other dielectric sheet of the core which comprises FEP Teflon material or polyethylene, which provide more desirable electrical characteristics.

The aforementioned triplate construction has several drawbacks: (1) it is not a true triplate configuration in which X-Y signal planes are disposed about a conductive power or reference plane (although true triplate constructions have been achieved by other fabrication techniques, they have not been successful in providing such constructions with low dielectric materials); (2) there is no teaching in the above-mentioned patent how vias can be fabricated between individual signal planes embedded as a core within the multi-laminated board structure; (3) it would be more desirable to replace the epoxy-glass resin layers of the patented structure with dielectric materials having lower dielectric constants, without jeopardizing the structural strength of the circuit board assembly; (4) if an electrical short should develop within any one of the cores of the assembly, the whole assembly must be discarded. Such electrical short circuits occur with greater prevalence in high performance circuit boards as layers become thinner and signal line density is increased.

The invention as claimed is intended to remedy these drawbacks.

The invention features a method of fabricating high performance printed circuit board assemblies comprising at least two laminated circuitized power plane sub-assemblies. The circuitized power plane sub-assemblies are modular in that they are fabricated in a prior assembly process, and then laminated to other assembly elements as a finished core unit.

One of the advantages to using this type of fabricating technique is that each modular unit can be tested for electrical integrity prior to its integration into the final assembly. Defective circuit board sub-assemblies can be discarded rather than having to discard the completed assembly, as with present techniques. The invention thus provides less waste, and improves reliability.

The assembly of the invention is of true triplate construction, consisting of two laminated sub-assemblies characterized by spaced-apart X-Y signal planes disposed about two internal power planes. Vias run through the core where necessary to provide communication between the X and Y signal planes.

The triplate core is prefabricated as follows:

(i) a first core comprising a sheet of an electrical conductor disposed on either side of a dielectric layer is circuitized with a power distribution pattern;

(ii) next, a second core is circuitized, the same as, or similar to the first;

(iii) the first and second cores are then laminated together with their power distribution patterns facing each other, in order to form a sub-assembly; and

(iv) the sub-assembly is then circuitized to provide a signal plane on either side thereof.

Plated vias are fabricated in the sub-assemblies where necessary.

The initial cores can have a layer of dielectric material with a low dielectric constant of less than 3.0, and preferably in the range of between 1.4 and 3.0. A suitable dielectric material for this purpose can comprise polytetrafluoroethylene.

Normally a core having a flexible dielectric such as polytetrafluoroethylene would be difficult to process into a finished sub-assembly, but the side sheets of conductive material, such as copper, lend structural stability to the core.

The modularization allows each sub-assembly to be fabricated at lower temperatures, despite the fact that the dielectric layers comprise polytetrafluoroethylene.

Still another advantage of the modular technique of the invention is provided by the greater choice of laminating materials. For example, it is intended to reduce the overall dielectric character

of the final assembly by laminating the sub-assemblies together using bonding films or a brominated epoxy resin, rather than a glass resin.

High performance is achieved by using the lower dielectrics, which in turn allows for thinner layers and increased wiring density.

These and other advantages and objectives will be better understood with reference to the following detailed description considered in conjunction with the accompanying drawings, in which

Figure 1 is a partial sectional view of a raw core for use in fabricating the modular sub-assembly of the invention;

Figure 2 shows a partial sectional view of the raw core of Figure 1, after being circuitized with a power pattern;

Figure 3 depicts a partial sectional view of an uncircuitized sub-assembly, formed by the lamination of two cores of the type illustrated in Figure 2;

Figure 4 is a partial sectional view of a finished sub-assembly; and

Figure 5 illustrates a final printed circuit board assembly utilizing within its construction two sub-assemblies of Figure 4, which have been laminated together.

In general, the printed circuit board of this invention is constructed using many of the same materials and processes outlined and described in US-A-4 448 804, which teaches a technique for plating copper to non-conductive surfaces, such as dielectric materials; US-A-4 030 190, which describes a method of forming multilayered printed circuit boards; and US-A-3 523 037, which illustrates a method of fabricating laminate boards that are used to construct multilayered assemblies.

For the sake of brevity, it is desired to incorporate herein, the teachings and description of these materials and processes from the aforementioned patents, all of which are hereby incorporated by reference.

Generally speaking, the invention pertains to a modular technique for fabricating high performance circuit board assemblies.

The assembly has a triplate geometry and comprises modular units having X and Y signal planes disposed on either side of two centralized power planes.

Each sub-assembly has its own vias communicating between the X and Y signal planes, such that when these modular units are laminated into the final circuit board assembly, these vias form internal communicating ducts.

For the purposes of clarity, like elements will have the same designation throughout the figures.

Now referring to Figure 1, a raw core is shown in partial sectional view by arrow 2. The raw core 2 is comprised of an inner layer 3 of a dielectric material having a low dielectric constant of less than 3.0, and preferably in a range of 1.4 to 3.0. Such a suitable material may be polytetrafluoroethylene. Layered on either side of layer 3 are copper sheets 4 and 5, respectively. In order to fabricate a modular sub-assembly 10 as shown in Figure 4, the raw core 2 is first etched on one of the two copper sides 4 or 5, respectively, with a power pattern 6, as illustrated in Figure 2.

This etching step is repeated for another similar raw core 2', which can be a mirror image of core 2. The two etched cores 2 and 2' are then laminated together, as shown in Figure 3, by means of a sticker sheet 7. Sheet 7 can comprise a bonding film or a brominated epoxy resin. A low dielectric bonding material is selected to reduce the overall dielectric character of the sub-assembly, shown by the bracket 10 in Figure 4. The cores 2 and 2' are bonded together with their respective power patterns 6 facing each other.

The sub-assembly 10 is achieved by circuitizing the outer sheets 4 of the laminated cores 2 and 2', respectively of Figure 3, with a respective X and Y signal pattern, as depicted in Figure 4. Appropriate vias 8 are formed in the sub-assembly 10 where needed.

The circuitizing of sheets 4 is accomplished by additive or subtractive techniques known in the art.

Referring to Figure 5, a final circuit board assembly is illustrated by arrow 20.

The circuit board assembly 20 comprises at least two sub-assemblies 10, as shown. Sub-assemblies 10 can be laminated together by a sticker sheet 7 of low dielectric-strength bonding material.

Reference planes 9 can be laminated about the joined sub-assemblies 10, and appropriate plated through-holes 11 will be added to complete assembly 20.

One of the advantages of constructing an assembly 20 by the modularized method of this invention is the ability to electrically test each sub-assembly 10 before it is laminated into the final circuit board assembly 20. In this manner, only defective sub-assemblies 10 are discarded, rather than entire assemblies 20.

Except for the special methodology of the modularized technique of this invention, all construction steps used herein are within the state of the art.

Lower temperature processes will become feasible despite the use of materials normally requiring high temperature processes. The use of thinner and more flexible materials will also be possible, with the use of the modularized technique of this invention.

The modularized sub-assemblies provide a greater structural stability to the fabrication, which would not ordinarily be possible with standard construction practices.

Claims

1. A high performance printed circuit board assembly (20), comprising at least two modular sub-assemblies (10) adjacently laminated together, each of said modular sub-assemblies characterized by a signal plane (4, 5) disposed on opposite sides of two internal power planes and electrically communicating by means of vias (8) formed within each respective sub-assembly.

2. The high performance printed circuit board assembly of claim 1, wherein each sub-assembly (10) is further characterized by a dielectric laminate (3) between each signal plane and an adjacent power plane having a dielectric constant of approximately less than 3.0, preferably between 1.4 and 3.0.

3. The high performance printed circuit board assembly of one of the preceding claims, wherein said dielectric laminate comprises polytetrafluoroethylene.

4. The high performance printed circuit board assembly of one of the preceding claims, wherein said two modular sub-assemblies are adjacently laminated together by a bonding film (7), preferably by a brominated epoxy resin.

5. A method of constructing a high performance printed circuit board assembly utilizing a modular construction technique comprising the steps of:
   (a) fabricating a number of circuitized power plane sub-assemblies, each respective sub-assembly characterized by a signal plane disposed on opposite sides of two internal power planes and electrically communicating by means of plated vias where necessary; and
   (b) laminating at least two sub-assemblies together to form a composite; and
   (c) constructing a printed circuit board assembly by building a multi-laminate structure using said composite.

6. The method of constructing a high performance printed circuit board assembly in accordance with claim 5, wherein the fabrication of each sub-assembly of step (a) further comprises the steps of:
   (i) circuitizing with a power distribution pattern one side of a first core comprising a sheet of an electrical conductor disposed on either side of a dielectric layer;
   (ii) circuitizing a second core similar to step (i);
   (iii) laminating said first and second cores together with said power distribution patterns facing each other to form a sub-assembly; and
   (iv) circuitizing said sub-assembly to provide a signal plane on either side thereof.

7. The method of constructing a high performance printed circuit board assembly, in accordance with claim 6, further comprising the step of:
   (v) fabricating plated vias in said sub-assembly where necessary.

8. The method of constructing a high performance printed circuit board assembly in accordance with one of the preceding claim 5 to 7, further comprising the step of:
   (d) testing each respective sub-assembly for electrical integrity prior to the laminating step (b).

9. The method of constructing a high performance printed circuit board assembly in accordance with one of the preceding claims 5 to 8, wherein said signal planes are fabricated about said power planes with a dielectric layer therebetween having a dielectric constant of approximately less than 3.0, preferably between 1.4 and 3.0.

10. The method of constructing a high performance printed circuit board assembly in accordance with claim 9, wherein said dielectric layer comprises polytetrafluoroethylene.

11. The method of constructing a high performance printed circuit board assembly in accordance with one of the preceding claims 5 to 10, wherein the laminating of the first and second cores together in step (iii) and/or the laminating step (b) includes the use of a bonding film, preferably a brominated epoxy resin.

Patentansprüche

1. Leiterplattenanordnung hoher Leistungsfähigkeit (20), die mindestens zwei aufeinander laminierte modulare Unteranordnungen (10) umfaßt, die beide durch je eine zu beiden gegenüber liegenden Seiten von zwei inneren Strom-

* C L M S *

The modularized sub-assemblies provide a greater structural stability to the fabrication, which would not ordinarily be possible with standard construction practices.

Claims

1. A high performance printed circuit board assembly (20), comprising at least two modular sub-assemblies (10) adjacently laminated together, each of said modular sub-assemblies characterized by a signal plane (4, 5) disposed on opposite sides of two internal power planes and electrically communicating by means of vias (8) formed within each respective sub-assembly.

2. The high performance printed circuit board assembly of claim 1, wherein each sub-assembly (10) is further characterized by a dielectric laminate (3) between each signal plane and an adjacent power plane having a dielectric constant of approximately less than 3.0, preferably between 1.4 and 3.0.

3. The high performance printed circuit board assembly of one of the preceding claims, wherein said dielectric laminate comprises polytetrafluoroethylene.

4. The high performance printed circuit board assembly of one of the preceding claims, wherein said two modular sub-assemblies are adjacently laminated together by a bonding film (7), preferably by a brominated epoxy resin.

5. A method of constructing a high performance printed circuit board assembly utilizing a modular construction technique comprising the steps of:
   (a) fabricating a number of circuitized power plane sub-assemblies, each respective sub-assembly characterized by a signal plane disposed on opposite sides of two internal power planes and electrically communicating by means of plated vias where necessary; and
   (b) laminating at least two sub-assemblies together to form a composite; and
   (c) constructing a printed circuit board assembly by building a multi-laminate structure using said composite.

6. The method of constructing a high performance printed circuit board assembly in accordance with claim 5, wherein the fabrication of each sub-assembly of step (a) further comprises the steps of:
   (i) circuitizing with a power distribution pattern one side of a first core comprising a sheet of an electrical conductor disposed on either side of a dielectric layer;
   (ii) circuitizing a second core similar to step (i);
   (iii) laminating said first and second cores together with said power distribution patterns facing each other to form a sub-assembly; and
   (iv) circuitizing said sub-assembly to provide a signal plane on either side thereof.

7. The method of constructing a high performance printed circuit board assembly, in accordance with claim 6, further comprising the step of:
   (v) fabricating plated vias in said sub-assembly where necessary.

8. The method of constructing a high performance printed circuit board assembly in accordance with one of the preceding claim 5 to 7, further comprising the step of:
   (d) testing each respective sub-assembly for electrical integrity prior to the laminating step (b).

9. The method of constructing a high performance printed circuit board assembly in accordance with one of the preceding claims 5 to 8, wherein said signal planes are fabricated about said power planes with a dielectric layer therebetween having a dielectric constant of approximately less than 3.0, preferably between 1.4 and 3.0.

10. The method of constructing a high performance printed circuit board assembly in accordance with claim 9, wherein said dielectric layer comprises polytetrafluoroethylene.

11. The method of constructing a high performance printed circuit board assembly in accordance with one of the preceding claims 5 to 10, wherein the laminating of the first and second cores together in step (iii) and/or the laminating step (b) includes the use of a bonding film, preferably a brominated epoxy resin.

Patentansprüche

1. Leiterplattenanordnung hoher Leistungsfähigkeit (20), die mindestens zwei aufeinander laminierte modulare Unteranordnungen (10) umfaßt, die beide durch je eine zu beiden gegenüber liegenden Seiten von zwei inneren Strom-

* C L M S *

versorgungsebenen und elektrisch durch in jeder Unteranordnung angebrachte Durchgangsverbindungen (8) verbundene Signalebene (4, 5) gekennzeichnet sind.

2. Leiterplattenanordnung hoher Leistungsfähigkeit nach Anspruch 1, bei der jede Unteranordnung (10) weiterhin durch ein dielektrisches Laminat (3) zwischen jeder signalebene und einer angrenzenden Stromversorgungsebene mit einer Dielektrizitätskonstanten von ungefähr kleiner als 3,0, vorzugsweise zwischen 1,4 und 3,0, gekennzeichnet ist.

3. Leiterplattenanordnung hoher Leistungsfähigkeit nach einem der vorhergehenden Ansprüche, bei der das dielektrische Laminat Polytetrafluorethylen umfaßt.

4. Leiterplattenanordnung hoher Leistungsfähigkeit nach einem der vorhergehenden Ansprüche, bei der die beiden Unteranordnungen durch eine Bondfolie (7), vorzugsweise durch ein bromiertes Epoxidharz, aufeinander laminiert werden.

5. Verfahren zum Aufbau einer Leiterplattenanordnung hoher Leistungsfähigkeit unter Verwendung eines modularen Bauprinzips, das die folgenden Schritte umfaßt:
   (a) Herstellung einer Anzahl von Unteranordnungen als Stromversorgungsebenen mit Schaltungsstruktur, wobei jede Unteranordnung durch je eine zu beiden Seiten von zwei inneren Stromversorgungsebenen angebrachte Signalebene und dort, wo es erforderlich ist, durch beschichtete, die Signalebenen elektrisch verbindenden Durchgangsverbindungen gekennzeichnet ist; und
   (b) Laminieren von mindestens zwei Unteranordnungen zusammen, um eine Verbundstruktur zu bilden; und
   (c) Herstellen einer Leiterplattenanordnung durch Erzeugen einer Mehrfachlaminatstruktur unter Verwendung dieser Verbundstruktur.

6. Verfahren zur Herstellung einer Leiterplattenanordnung hoher Leistungsfähigkeit nach Anspruch 5, bei dem die Fertigung jeder Unteranordnung in Schritt (a) die folgenden Schritte umfaßt:
   (i) Erzeugen einer Stromversorgungs-Schaltungsstruktur auf einer Seite einer ersten Kernstruktur, die eine Folie aus einem elektrischen Leiter zu beiden Seiten einer dielektrischen Schicht umfaßt;
   (ii) Erzeugen einer Schaltungsstruktur auf einer zweiten Kernstruktur wie in Schritt (i);
   (iii) Laminieren der ersten und zweiten Kernstruktur zusammen mit den einander gegenüberliegenden Stromversorgungsstrukturen, so daß eine Unteranordnung entsteht; und
   (iv) Erzeugen einer Schaltungsstruktur auf der Unteranordnung, damit auf beiden Steiten der Unteranordnung eine Signalebene entsteht.

7. Verfahren zum Aufbau einer Leiterplattenanordnung hoher Leistungsfähigkeit nach Anspruch 6, das weiterhin den Schritt des:
   (v) Herstellens beschichteter Durchgangsverbindungen dort, wo es erforderlich ist, umfaßt.

8. Verfahren zum Aufbau einer Leiterplattenanordnung hoher Leistungsfähigkeit nach einem der vorhergehenden Ansprüche 5 bis 7, das weiterhin den Schritt der:
   (d) Prüfung jeder Unteranordnung auf elektrische Unversehrtheit vor dem Laminierschritt (b) umfaßt.

9. Verfahren zur Herstellung einer Leiterplattenanordnung hoher Leistungsfähigkeit nach einem der vorhergehenden Ansprüche 5 bis 8, bei dem die Signalebenen auf den Stromversorgungsebenen mit einer dazwischenliegenden dielektrischen Schicht hergestellt werden, die eine Dielektrizitätskonstante von ungefähr kleiner als 3,0, vorzugsweise zwischen 1,4 und 3,0, hat.

10. Verfahren zur Herstellung einer Leiterplattenanordnung hoher Leistungsfähigkeit nach Anspruch 9, bei dem die dielektrische Schicht Polytetrafluorethylen umfaßt.

11. Verfahren zur Herstellung einer Leiterplattenanordnung hoher Leistungsfähigkeit nach einem der vorhergehenden Ansprüche 5 bis 10, bei dem das Aufeinanderlaminieren der ersten und zweiten Kernstruktur in Schritt (iii) und/oder Schritt (b) die Verwendung einer Bondfolie, vorzugsweise eines bromierten Epoxidharzes, beinhaltet.

Revendications

1. Ensemble de plaquettes à circuit imprimé à performance élevée (20) comprenant au moins deux sous-ensembles modulaires (10) laminés ensemble de façon adjacente, chacun desdits sous-ensembles modulaires étant caractérisé par un plan de signal (4, 5) disposé sur les

* C L M S *

côtés opposés de deux plans d'énergie internes et communiquant électriquement au moyen de passages (8) formés dans chaque sous-ensemble respectif.

2. Ensemble de plaquettes à circuit imprimé à performance élevée selon la revendication 1, dans lequel chaque sous-ensemble (10) est en outre caractérisé par une stratification (3) entre chaque plan de signal et un plan d'énergie adjacent ayant une constante diélectrique approximativement inférieure à 3,0, de préférence entre 1,4 et 3,0.

3. Ensemble de plaquettes à circuit imprimé à performance élevée selon l'une ou l'autre des revendications précédentes, dans lequel ladite stratification diélectrique est du polytétrafluoroéthylène.

4. Ensemble de plaquettes à circuit imprimé à performance élevée selon l'une quelconque des revendications précédentes, dans lequel lesdits deux sous-ensembles modulaires sont laminés ensemble de façon adjacente par un film de liaison (7), de préférence, par une résine époxy bromée.

5. Ensemble de plaquettes à circuit imprimé à performance élevée utilisant une technique de construction modulaire comprenant les étapes de:

(a) fabriquer un nombre de sous-ensembles de plans d'énergie avec circuit, chaque sous-ensemble respectif étant caractérisé par un plan de signal disposé sur les côtés opposés de deux plans d'énergie internes et communiquant électriquement au moyen de passages plaqués là où c'est nécessaire; et

(b) laminer ensemble au moins deux sous-ensembles pour former un composite; et

(c) construire un ensemble de plaquettes à circuit imprimé en établissant une structure à couches multiples utilisant ledit composite.

6. Procédé de construction d'un ensemble de plaquettes à circuit imprimé conformément à la revendication 5, dans lequel la fabrication de chaque sous-ensemble de l'étape (a) comprend en outre les étapes de:

(i) former un circuit avec une configuration de répartition d'énergie sur un côté d'un premier tore comprenant une feuille de conducteur électrique disposée de chaque côté d'une couche diélectrique;

(ii) former un circuit sur un deuxième tore similaire à l'étape (i);

(iii) laminer lesdits premier et deuxième tores ensemble avec lesdites configurations de répartition d'énergie se faisant face pour former un sous-ensemble; et

(iv) former un circuit sur ledit sous-ensemble pour fournir un plan de signal sur chacun de ses côtés.

7. Procédé de construction d'un ensemble de plaquettes à circuit imprimé à performance élevée conformément à la revendication 6, comprenant en outre l'étape de:

(v) fabriquer des passages plaqués dans ledit sous-ensemble là où c'est nécessaire.

8. Procédé de construction d'un ensemble de plaquettes à circuit imprimé à performance élevée conformément à l'une quelconques des revendications précédentes 5 à 7, comprenant en outre l'étape de:

(d) tester chaque sous-ensemble respectif pour l'intégrité électrique avant l'étape de laminer (b).

9. Procédé de construction d'un ensemble de plaquettes à circuit imprimé à performance élevée conformément à l'une quelconque des revendications précédentes 5 à 8, dans lequel lesdits plans de signal sont fabriqués sur les côtés desdits plans d'énergie avec une couche diélectrique entre eux ayant une constante diélectrique approximativement inférieure à 3,0, de préférence, entre 1,4 et 3,0.

10. Procédé de construction d'un ensemble de plaquettes à circuit imprimé à performance élevée conformément à la revendication 9, dans lequel ladite couche diélectrique est du polytétrafluoroéthylène.

11. Procédé de construction d'un ensemble de plaquettes à circuit imprimé conformément à l'une des revendications précédentes 5 à 10, dans lequel la stratification des premier et deuxième tores ensemble dans l'étape (iii) et/ou l'étape de stratification (b) comprend l'utilisation d'un film de liaison, de préférence, une résine époxy bromée.