

CORRECTED VERSION

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
25 July 2013 (25.07.2013)



(10) International Publication Number
WO 2013/107779 A8

(51) International Patent Classification:
G11C 7/06 (2006.01) *G11C 7/12* (2006.01)
G11C 11/4091 (2006.01)

(21) International Application Number:
PCT/EP2013/050760

(22) International Filing Date:
16 January 2013 (16.01.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1250398 16 January 2012 (16.01.2012) FR

(71) Applicant: SOITEC [FR/FR]; Chemin des Franques, F-38190 Bernin (FR).

(72) Inventors: FERRANT, Richard; Village de Suguensou, F-29770 Esquibien (FR). THEWES, Roland; Zum Kiefernwald 2, D-14532 Kleinmachnow (DE).

(74) Agent: REGIMBEAU; 20 rue de Chazelles, F-75847 Paris Cedex 17 (FR).

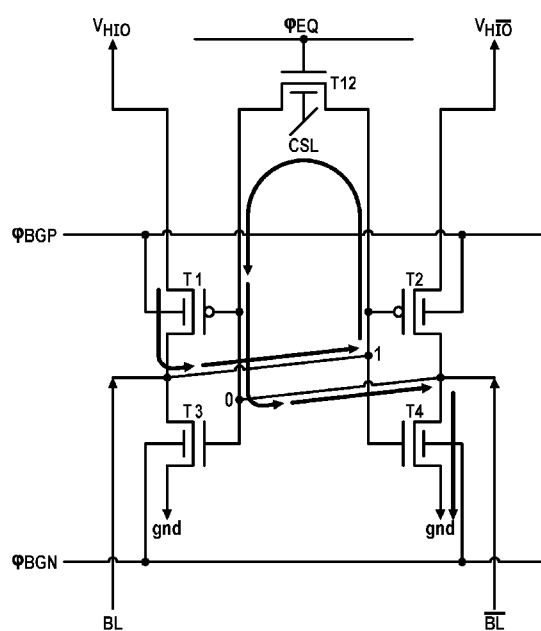
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,

[Continued on next page]

(54) Title: CIRCUIT AND METHOD FOR SENSING A DIFFERENCE IN VOLTAGE ON A PAIR OF DUAL SIGNAL LINES, IN PARTICULAR THROUGH EQUALIZE TRANSISTOR

FIG. 5



(57) Abstract: The invention relates to a circuit for sensing a difference in voltage on a pair of dual signal lines comprising a first signal line (BL) and a second signal line (/BL) complementary to the first signal line, comprising: - a pair of cross-coupled inverters arranged between the first and the second signal lines, each inverter having a pull-up transistor (T1, T2) and a pull-down transistor (T3, T4), the sources of the pull-up transistors or of the pull-down transistors being respectively connected to a first (V_{HIO}) and a second (V_{HIO}) pull voltage signals, - a decode transistor (T11, T12) having source and drain terminals respectively coupled to one of the first and second signal lines and a gate controlled by a decoding control signal (CSL), whereby when the decode transistor is turned on by the decoding control signal, a short circuit is established between the first and the second signal lines through which current flows from one of the first and second pull voltage signals, thereby generating a disturb in between the first and the second pull voltage signals.



EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

(48) Date of publication of this corrected version:

13 February 2014

(15) Information about Correction:

see Notice of 13 February 2014

Published:

— *with international search report (Art. 21(3))*