CLAIMS

We claim:

1. A computing system comprising:

a battery to supply power to the computing system;

a processor to run an operating system (OS);

a basic input/output system (BIOS) comprising:

an interceptor to assume control over the processor in response to an OS request to transition the processor into a sleeping state;

a transitioner to transition the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

a wake unit to maintain the processor in the intermediate state until a wake event is detected.

2. The computing system of claim 1, wherein the BIOS further includes a resume unit to reverse one or more power lowering operations in response to the wake event.

3. The computing system of any one of claims 1 or 2, wherein the transitioner includes:

a state clearer to conduct a reset of the processor;

a resume unit to perform one or more processor resume operations;

a processor power saver to perform one or more processor power lowering operations; and

a handoff unit to transfer control over the processor to the OS in response to a wake event.

4. The computing system of claim 3, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

5. The computing system of any one of claims 1 or 2, wherein the transitioner includes:

a device power saver to perform one or more device power lowering operations; and

a processor power saver to perform one or more processor power lowering operations.

6. The computing system of claim 5, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state.

7. A method of operating a basic input/output system (BIOS), comprising:

assuming control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

transitioning the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

maintaining the processor in the intermediate state until a wake event is detected.

8. The method of claim 7, further including reversing one or more power lowering operations in response to the wake event.

9. The method of any one of claims 7 or 8, wherein transitioning the processor into the intermediate state includes:

conducting a reset of the processor;

performing one or more processor resume operations;

performing one or more processor power lowering operations; and

transferring control over the processor to the OS.

10. The method of claim 9, wherein the sleeping state is an Advanced Configuration and Power Interface (ACPI) S3 state.

11. The method any one of claims 7 or 8, wherein transitioning the processor into the intermediate state includes:

performing one or more device power lowering operations; and

performing one or more processor power lowering operations.

12. The method of claim 11, wherein the sleeping state is an Advanced Configuration and Power Interface (ACPI) S1 state.

13. At least one computer readable storage medium comprising a set of basic input/output system (BIOS) instructions which, when executed by a computing system, cause the computing system to:

assume control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

transition the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

maintain the processor in the intermediate state until a wake event is detected.

14. The at least one computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to reverse one or more power lowering operations in response to the wake event.

15. The at least one computer readable storage medium of any one of claims 13 or 14, wherein the BIOS instructions, when executed, cause a computing system to:

conduct a reset of the processor;

perform one or more processor resume operations;

perform one or more processor power lowering operations; and

transfer control over the processor to the OS.

16. The at least one computer readable storage medium of claim 15, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

17. The at least one computer readable storage medium of any one of claims 13 or 14, wherein the BIOS instructions, when executed, cause a computing system to:

perform one or more device power lowering operations; and

perform one or more processor power lowering operations.

18. The at least one computer readable storage medium of claim 17, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state.

19. A basic input/output system (BIOS) apparatus comprising:

an interceptor to assume control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

a transitioner to transition the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

a wake unit to maintain the processor in the intermediate state until a wake event is detected.

20. The apparatus of claim 19, further including a resume unit to reverse one or more power lowering operations in response to the wake event.

21. The apparatus of any one of claims 19 or 20, wherein the transitioner includes:

a state clearer to conduct a reset of the processor;

a resume unit to perform one or more processor resume operations;

a processor power saver to perform one or more processor power lowering operations; and

a handoff unit to transfer control over the processor to the OS.

22. The apparatus of claim 21, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

23. The apparatus of any one of claims 19 or 20, wherein the transitioner includes:

a device power saver to perform one or more device power lowering operations; and

a processor power saver to perform one or more processor power lowering operations.

24. The apparatus of claim 23, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state.

25. A basic input/output system (BIOS) apparatus comprising:

means for assuming control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

means for transitioning the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

means for maintaining the processor in the intermediate state until a wake event is detected.

CLAIMS

We claim:

1. A computing system comprising:

a battery to supply power to the computing system;

a processor to run an operating system (OS);

a basic input/output system (BIOS) comprising:

an interceptor to assume control over the processor in response to an OS request to transition the processor into a sleeping state;

a transitioner to transition the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

a wake unit to maintain the processor in the intermediate state until a wake event is detected.

2. The computing system of claim 1, wherein the BIOS further includes a resume unit to reverse one or more power lowering operations in response to the wake event.

3. The computing system of any one of claim 1, wherein the transitioner includes:

a state clearer to conduct a reset of the processor;

a resume unit to perform one or more processor resume operations;

a processor power saver to perform one or more processor power lowering operations; and

a handoff unit to transfer control over the processor to the OS in response to a wake event.

4. The computing system of claim 3, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

5. The computing system of any one of claim 1, wherein the transitioner includes:

a device power saver to perform one or more device power lowering operations; and

a processor power saver to perform one or more processor power lowering operations.

6. The computing system of claim 5, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state.

7. A method of operating a basic input/output system (BIOS), comprising:

assuming control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

transitioning the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

maintaining the processor in the intermediate state until a wake event is detected.

8. The method of claim 7, further including reversing one or more power lowering operations in response to the wake event.

9. The method of any one of claim 7, wherein transitioning the processor into the intermediate state includes:

conducting a reset of the processor;

performing one or more processor resume operations;

performing one or more processor power lowering operations; and

transferring control over the processor to the OS.

10. The method of claim 9, wherein the sleeping state is an Advanced Configuration and Power Interface (ACPI) S3 state.

11. The method any one of claim 7, wherein transitioning the processor into the intermediate state includes:

performing one or more device power lowering operations; and

performing one or more processor power lowering operations.

12. The method of claim 11, wherein the sleeping state is an Advanced Configuration and Power Interface (ACPI) S1 state.

13. At least one computer readable storage medium comprising a set of basic input/output system (BIOS) instructions which, when executed by a computing system, cause the computing system to:

assume control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

transition the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

maintain the processor in the intermediate state until a wake event is detected.

14. The at least one computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to reverse one or more power lowering operations in response to the wake event.

15. The at least one computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to:

conduct a reset of the processor;

perform one or more processor resume operations;

perform one or more processor power lowering operations; and

transfer control over the processor to the OS.

16. The at least one computer readable storage medium of claim 15, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

17. The at least one computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to:

perform one or more device power lowering operations; and

perform one or more processor power lowering operations.

18. The at least one computer readable storage medium of claim 17, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state.

19. A basic input/output system (BIOS) apparatus comprising:

an interceptor to assume control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

a transitioner to transition the processor into an intermediate state that has a shorter wake latency than the sleeping state; and

a wake unit to maintain the processor in the intermediate state until a wake event is detected.

20. The apparatus of claim 19, further including a resume unit to reverse one or more power lowering operations in response to the wake event.

21. The apparatus of claim 19, wherein the transitioner includes:

a state clearer to conduct a reset of the processor;

a resume unit to perform one or more processor resume operations;

a processor power saver to perform one or more processor power lowering operations; and

a handoffunit to transfer control over the processor to the OS.

22. The apparatus of claim 21, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

23. The apparatus of claim 19, wherein the transitioner includes:

a device power saver to perform one or more device power lowering operations; and

a processor power saver to perform one or more processor power lowering operations.

24. The apparatus of claim 23, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state.