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(71) Applicant *(for all designated States except US)*: **ACM RESEARCH, INC.** [US/US]; Suite 610, 46520 Fremont Boulevard, Fremont, CA 94538 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **YAO, Xiang, Yu** [US/US]; 1043 Ridgemond Drive, Milpitas, CA 95035 (US). **CHANG, Ru, Kao** [US/US]; 397 Preston Drive, MOuntain View, CA 94040 (US). **YIH, Peihaur** [—/US]; 37171 Sycamore Street #824, Newark, CA 94560 (US). **WANG, Hui** [CN/US]; 38855 Litchfield Circle, Fremont, CA 94536 (US).

(74) Agents: **YIM, Peter, J.** et al.; Morrison & Foerster LLP, 435 Market Street, San Francisco, CA 94105-2482 (US).

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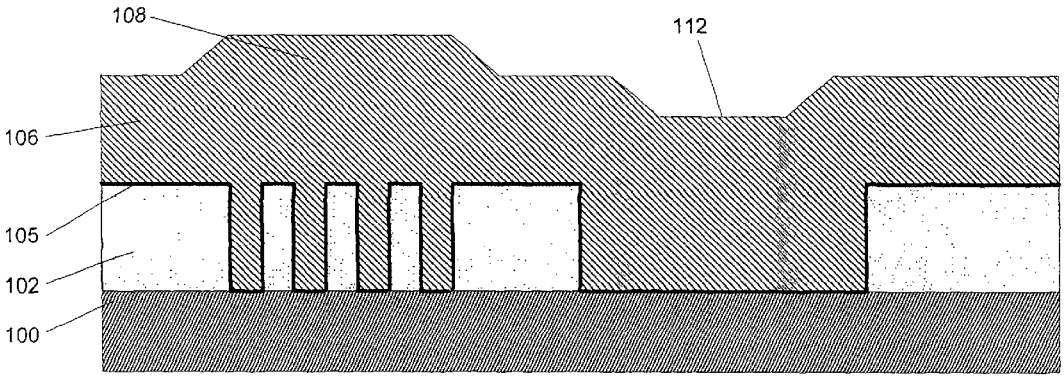
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(54) Title: FORMING A SEMICONDUCTOR STRUCTURE USING A COMBINATION OF PLANARIZING METHODS AND ELECTROPOLISHING



(57) Abstract: A method for planarizing and electropolishing a conductive layer on a semiconductor structure includes forming a dielectric layer with recessed areas and non-recessed areas on the semiconductor wafer. A conductive layer is formed over the dielectric layer to cover the recessed areas and non-recessed areas. The surface of the conductive layer is then planarized to reduce variations in the topology of the surface. The planarized conductive layer is then electropolished to expose the non-recessed area.

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