CLAIMS

What is claimed is:

1. A method for fabricating an integrated circuit comprising:

depositing a dielectric layer defining a plane;

etching the dielectric layer to form trenches;

depositing a ruthenium-containing liner layer overlying the dielectric layer;

filling the trenches with copper-containing metal;

recessing the copper-containing metal in each trench to form a space between the copper-containing metal and the plane;

filling the space with a capping layer; and

planarizing the layers to at least the plane.

2. The method of claim 1 further comprising depositing a barrier layer overlying the dielectric layer before depositing the ruthenium-containing liner layer.

3. The method of claim 1 further comprising depositing a barrier layer overlying the dielectric layer before depositing the ruthenium-containing liner layer, wherein the barrier layer comprises tantalum and tantalum nitride.

4. The method of claim 1 wherein filling the space with a capping layer comprises selectively depositing a capping layer selected from cobalt, manganese, and cobalt-tungsten-phosphorus onto the copper-containing metal.

5. The method of claim 4 wherein selectively depositing the capping layer on the copper-containing metal comprises selectively depositing cobalt or manganese onto the copper-containing metal by chemical vapor deposition.

6. The method of claim 4 wherein selectively depositing the capping layer on the copper-containing metal comprises depositing cobalt-tungsten-phosphorus onto the copper-containing metal by electroless deposition.

7. The method of claim 1 wherein filling the space with a capping layer comprises non-selectively depositing a capping layer selected from tantalum, titanium, tantalum-titanium, and dielectric material overlying the ruthenium-containing liner layer and the copper-containing metal.

8. The method of claim 1 wherein filling the trenches with copper-containing metal comprises depositing the copper-containing metal overlying the ruthenium-containing liner layer, and wherein the method further comprises planarizing the copper-containing metal to the ruthenium-containing liner layer before recessing the copper-containing metal in the trenches.

9. The method of claim 1 wherein planarizing the layers comprises planarizing the layers by chemical mechanical planarization to between the plane and the copper-containing metal.

10. A method for fabricating an integrated circuit comprising:

providing a partially fabricated integrated circuit including a dielectric layer formed with trenches having openings, a ruthenium-containing liner layer overlying the dielectric layer, and a copper-containing metal in the trenches;

capping the copper-containing metal with a capping layer; and

planarizing the partially fabricated integrated circuit to remove the ruthenium-containing liner layer between trenches, a portion of the dielectric layer between trenches, and a portion of the capping layer.

11. The method of claim 10 wherein capping the copper-containing metal with a capping layer comprises selectively depositing a capping layer selected from cobalt, manganese, and cobalt-tungsten-phosphorus onto the copper-containing metal in the trenches.

12. The method of claim 10 wherein capping the copper-containing metal with a capping layer comprises non-selectively depositing a capping layer selected from tantalum, titanium, tantalum-titanium, and dielectric material onto the copper-containing metal in the trenches and overlying the ruthenium-containing liner layer.

13. The method of claim 10 wherein capping the copper-containing metal with a capping layer comprises:

recessing the copper-containing metal to form a space between the copper-containing metal and the opening of each trench; and

filling the space with the capping layer.

14. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises providing a partially fabricated integrated circuit including a barrier layer between the dielectric layer and the ruthenium-containing liner layer.

15. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises providing a partially fabricated integrated circuit including a barrier layer comprised of tantalum and tantalum nitride between the dielectric layer and the ruthenium-containing liner layer.

16. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises depositing the capping metal overlying the ruthenium-containing liner layer and planarizing the capping metal to the ruthenium-containing liner layer.

17. The method of claim 16 wherein capping the copper-containing metal with a capping layer comprises:

etching the copper-containing metal with ammonium hydroxide, hydrogen peroxide, and deionized water followed by citric acid or diluted hydrofluoric acid to form a space between the copper-containing metal and the opening of each trench; and

filling the space with the capping layer.

18. A method for fabricating an integrated circuit comprising:

forming a metal interconnect structure including copper bounded by a ruthenium liner and positioned in a dielectric layer;

encapsulating the copper by depositing a capping layer over the copper; and

planarizing a portion of the capping layer, a portion of the dielectric material, and portions of the ruthenium liner not adjacent the metal interconnect structure.

19. The method of claim 18 wherein forming a metal interconnect structure comprises forming a barrier liner between the ruthenium liner and the dielectric layer.

20. The method of claim 18 further comprising recessing the copper to form a space over the copper and bounded by the ruthenium liner, and wherein encapsulating the copper comprises depositing the capping layer into the space.

CLAIMS

1. A method for fabricating an integrated circuit comprising:

depositing a dielectric layer having an upper surface defining a plane;

etching the dielectric layer to form trenches defined by trench surfaces;

depositing a ruthenium-containing liner layer overlying the dielectric layer;

filling the trenches with copper-containing metal;

recessing the copper-containing metal in each trench to form a space between the copper-containing metal and the plane while the ruthenium-containing liner layer covers the upper surface of the dielectric layer adjacent each trench;

filling the space with a capping layer; and

planarizing the layers to at least the plane.

2. The method of claim 1 further comprising depositing a barrier layer overlying the trench surfaces of the dielectric layer and directly on the upper surface of the dielectric layer before depositing the ruthenium-containing liner layer.

3. The method of claim 1 further comprising depositing a barrier layer overlying the trench surfaces of the dielectric layer and directly on the upper surface of the dielectric layer before depositing the ruthenium-containing liner layer, wherein the barrier layer comprises tantalum and tantalum nitride.

4. The method of claim 1 wherein filling the space with a capping layer comprises selectively depositing a capping layer selected from cobalt, manganese, and cobalt-tungsten-phosphorus onto the copper-containing metal.

5. The method of claim 4 wherein selectively depositing the capping layer on the copper-containing metal comprises selectively depositing cobalt or manganese onto the copper-containing metal by chemical vapor deposition.

6. The method of claim 4 wherein selectively depositing the capping layer on the copper-containing metal comprises depositing cobalt-tungsten-phosphorus onto the copper-containing metal by electroless deposition.

7. The method of claim 1 wherein filling the space with a capping layer comprises non-selectively depositing a capping layer selected from tantalum, titanium, tantalum-titanium, and dielectric material overlying the ruthenium-containing liner layer and the copper-containing metal.

8. The method of claim 1 wherein filling the trenches with copper-containing metal comprises depositing the copper-containing metal overlying the ruthenium-containing liner layer, and wherein the method further comprises planarizing the copper-containing metal to the ruthenium-containing liner layer before recessing the copper-containing metal in the trenches.

9. The method of claim 1 wherein depositing a ruthenium-containing liner layer overlying the dielectric layer comprises forming trench portions of the ruthenium-containing liner overlying the trench surfaces of the dielectric layer and a trench adjacent portions of the ruthenium-containing liner overlying the upper surface of the dielectric layer; and wherein filling the trenches with copper-containing metal comprises depositing the copper-containing metal overlying the trench portions and the trench adjacent portions of the ruthenium-containing liner.

10. A method for fabricating an integrated circuit comprising:

providing a partially fabricated integrated circuit including a dielectric layer formed with trenches having openings, a ruthenium-containing liner layer overlying the dielectric layer, and a copper-containing metal in the trenches;

capping the copper-containing metal with a capping layer; and

planarizing the partially fabricated integrated circuit to remove the ruthenium-containing liner layer between trenches, a portion of the dielectric layer between trenches, and a portion of the capping layer.

11. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises providing the dielectric layer with an upper surface between the openings, and wherein the method further comprises covering the upper surface of the dielectric layer

between the openings with the ruthenium-containing liner while capping the copper-containing metal with a capping layer.

12. The method of claim 10 wherein capping the copper-containing metal with a capping layer comprises non-selectively depositing a capping layer selected from tantalum, titanium, tantalum-titanium, and dielectric material onto the copper-containing metal in the trenches and overlying the ruthenium-containing liner layer.

13. The method of claim 10 wherein capping the copper-containing metal with a capping layer comprises:

recessing the copper-containing metal to form a space between the copper-containing metal and the opening of each trench; and

filling the space with the capping layer.

14. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises providing a partially fabricated integrated circuit including a dielectric layer formed with trenches having openings and an upper surface between the openings, and a barrier layer between the dielectric layer and the ruthenium-containing liner layer, wherein the barrier layer is formed directly on the upper surface of the dielectric layer.

15. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises providing a partially fabricated integrated circuit including a dielectric layer formed with trenches having openings and an upper surface between the openings, and a barrier layer comprised of tantalum and tantalum nitride between the dielectric layer and the ruthenium-containing liner layer, wherein the barrier layer is formed directly on the upper surface of the dielectric layer.

16. The method of claim 10 wherein providing a partially fabricated integrated circuit comprises depositing the capping metal overlying the ruthenium-containing liner layer and planarizing the capping metal to the ruthenium-containing liner layer.

17. The method of claim 16 wherein capping the copper-containing metal with a capping layer comprises:

etching the copper-containing metal with ammonium hydroxide, hydrogen peroxide, and deionized water followed by citric acid or diluted hydrofluoric acid to form a space between the copper-containing metal and the opening of each trench; and

filling the space with the capping layer.

18. A method for fabricating an integrated circuit comprising:

forming a metal interconnect structure including copper bounded by a ruthenium liner and positioned in a dielectric layer;

encapsulating the copper by depositing a capping layer over the copper; and

planarizing a portion of the capping layer, a portion of the dielectric material, and portions of the ruthenium liner outside the metal interconnect structure.

19. The method of claim 18 wherein the dielectric layer has an upper surface adjacent the metal interconnect structure, and wherein forming a metal interconnect structure comprises forming a barrier liner between the ruthenium liner and the dielectric layer, wherein a portion of the barrier liner is formed on the upper surface of the dielectric layer.

20. The method of claim 18 wherein the dielectric layer has an upper surface adjacent the metal interconnect structure, and further comprising covering the upper surface of the dielectric layer with the portions of the ruthenium-containing liner outside the metal interconnect structure while encapsulating the copper by depositing a capping layer over the copper.

21. An integrated circuit fabricated in accordance with any one of the preceding claims.