**WHAT IS CLAIMED IS:**

1. A semiconductor system comprising:

a semiconductor device configured to output a temperature code corresponding to an internal temperature thereof; and

a controller configured to control, based on the temperature code, the semiconductor device to set a temperature measurement mode among at least two temperature measurement modes having different required times each for measuring the internal temperature and to measure the internal temperature in the set temperature measurement mode.

2. The semiconductor system of claim 1, wherein the controller comprises:

a command generator configured to generate a temperature measurement command for controlling the semiconductor device to measure the internal temperature; and

a mode setting component configured to receive the temperature code from the semiconductor device and control an operation of the command generator according to the temperature code.

3. The semiconductor system of claim 2, wherein the mode setting component comprises:

a threshold value storage configured to store a threshold value; and

a comparator configured to compare the threshold value with the temperature code to output a signal indicating whether the temperature code is less than the threshold value.

4. The semiconductor system of claim 1, wherein the semiconductor device comprises:

a temperature sensor configured to measure the internal temperature and generate at least one pulse corresponding to the internal temperature;

a pulse counter configured to count the at least one pulse to generate and output pulse information; and

a temperature code generator configured to receive a temperature measurement command indicating the set temperature measurement mode from the controller, and generate the temperature code based on the pulse information in response to the temperature measurement command.

5. The semiconductor system of claim 4, wherein the semiconductor device further comprises a mode register configured to store a value corresponding to the temperature measurement command.

6. The semiconductor system of claim 5,

wherein the semiconductor device further comprises a first

temperature code table and a second temperature code table, and

wherein the temperature code generator generates the temperature code by referring to the first temperature code table or the second temperature code table according to the pulse information and the value stored in the mode register.

7. The semiconductor system of claim 6, wherein the first temperature code table or the second temperature code table includes at least one temperature code corresponding to the pulse information.

8. The semiconductor system of claim 5, wherein the pulse information includes the number of pulses output from the pulse counter.

9. The semiconductor system of claim 5, wherein the pulse information includes a width of the pulse output from the pulse counter.

10. The semiconductor system of claim 1,

wherein the at least two temperature measurement modes include a short mode and a long mode, and

wherein a time required for measuring the internal temperature of the short mode is shorter than a time required for measuring the internal temperature of the long mode.

11. The semiconductor system of claim 10, wherein the short mode is set to represent the temperature code with a lesser number of bits than the number of bits of the long mode.

12. The semiconductor system of claim 10, wherein the controller controls the semiconductor device to set the short mode at a temperature lower than a temperature at which the long mode is set.

13. The semiconductor system of claim 10,

wherein the controller controls the semiconductor device to set the short mode in a first temperature range and to set the long mode in a second temperature range, and

wherein the first temperature range is lower than the second temperature range.

14. A storage device comprising:

a memory device including a memory cell that stores data and configured to perform an operation on the memory cell; and

a memory controller configured to control a length of a first period during which the operation is performed and a length of a second period during which a temperature measurement operation of measuring an internal temperature of the memory device is performed based on the internal temperature of the memory device,

wherein the memory controller sets a mode of the temperature measurement operation among at least two modes having different

required times each for measuring the internal temperature, and

wherein the memory device performs the temperature measurement operation in the mode.

15. The storage device of claim 14,

wherein the memory device comprises a temperature measurer configured to perform the temperature measurement operation in a short mode or a long mode,

wherein each of the short mode and the long mode includes the first period and the second period, and

wherein the length of the second period in the short mode is shorter than the length of the second period in the long mode.

16. The storage device of claim 14, wherein the operation includes at least one of a program operation, a read operation, and an erase operation.

17. The storage device of claim 14, wherein the operation includes at least one of an input/output operation of the data and a refresh operation.

18. The storage device of claim 15, wherein the temperature measurer performs the measurement in the short mode when a temperature code generated as a result of performing the temperature measurement operation is less than a threshold value.

19. The storage device of claim 18, wherein the temperature code includes a value corresponding to the internal temperature.

20. The storage device of claim 15, wherein the temperature measurer performs the temperature measurement operation in the short mode at a temperature lower than a temperature at which the temperature measurer performs the temperature measurement operation in the long mode.

21. A memory device comprising:

a memory cell array; and

a temperature sensor configured to measure an internal temperature of the memory cell array and generate at least one pulse corresponding to the internal temperature;

a pulse counter configured to evaluate the pulse and output pulse information corresponding thereto;

a temperature code generator configured to generate a temperature code corresponding to the pulse information; and

a mode register indicating an operation mode of the temperature sensor,

wherein the operation mode includes a short mode in which an operation time of the pulse counter is relatively short and a long mode in which the operation time of the pulse counter is relatively long, and

wherein the pulse counter counts the at least one pulse or measures a width of the pulse.

22. The memory device of claim 21, wherein the temperature sensor operates in the short mode when the internal temperature is relatively low, and operates in the long mode when the internal temperature is relatively high.

23. An operating method of a memory system including a controller and a memory device, the operating method comprising:

providing, by the memory device, the controller with information of a current temperature of the memory device;

determining, by the controller, a subsequent temperature sensing mode among at least two subsequent temperature sensing modes having different required times each for sensing a subsequent temperature of the memory device based on the current temperature; and

controlling, by the controller, the memory device to sense the subsequent temperature of the memory device in the determined subsequent temperature sensing mode.