

LINEAR TRANSCONDUCTOR

BACKGROUND OF THE INVENTION1. FIELD OF THE INVENTION

This invention relates to improvements in semiconductor circuits and methods, and more particularly to improvements in transconductance amplifiers suitable for use in closed loop automatic gain control circuits.

2. RELEVANT BACKGROUND

Transconductance amplifiers are well known in the art. In a typical transconductance amplifier, the differential input voltage is applied to the gates of MOS devices in series current paths that include current sourcing transistors and load transistors. Circuitry is also provided to insure that the gate-source voltage on the input devices is constant, in order to provide the linearity of the transconductance amplifier.

However, such transconductance amplifiers typically have a limited common-mode operating voltage range. For example, a typical prior art circuit is shown in Figure 1, to which reference is now made. Because the drain voltages of input transistors M1 and M2 are determined by transistor pairs M5-M3 and M6-M4, respectively, normally transistor M3 would be designed with a small $V_{gs}-V_{tn}$, whereas transistor M5 would have a bigger $V_{gs}-V_{tn}$. The drain voltage of transistor M1 is designed such that the current source transistor barely saturates, all in the weak corner. In the strong corner, the $V_{gs}-V_{tn}$ of transistor M3 and especially transistor M5 reduce by a factor of two; hence, drain voltage of transistor M1 becomes substantially lower. To

9903764-0

04 AUG 1999

keep transistor M1 operating in the saturated region, the voltage at input terminal p₂ (at the gate of transistor M1) would have to be at least V_{tn} above the drain voltage of transistor M1, and, hence becomes lowered as much as the drain voltage of transistor M1.

Ideally, the transconductance does not depend either on the input DC component or on the common-mode voltage. However, in the circuit of Figure 1, the transconductance is varied if either the input common-mode voltage varies or the input differential DC component is nonzero. This is especially undesirable in a filter applications that include multiple such transconductors that are controlled by the same MOSFET-resistor gate voltage which have cumulative DC offsets, or with different common-mode voltages, because the ratio of transconductances are not maintained at their designed values. Such problem is typical of any transconductor that drops level-shifted input voltages across a MOSFET-resistor to generate current.

Moreover, the circuit of Figure 1 produces large distortion if the differential amplitude or DC components of the input signal are larger than, for example, 200mV. This is especially so at the lowest end of the transconductance tuning range, where the $V_{gs}-V_{tn}$ of the MOSFET resistor is smallest, possibly less than 200mV. This again is typical of any transconductor that drops level-shifted input voltages across MOSFET-resistor to generate current.

What is needed, therefore, is a transconductor, or transconductance amplifier, which controls the V_{cc} input such that the common-mode voltage of the current source transistors are maintained at a predetermined voltage in

spite of manufacturing process variations, which maintains the ratio of transconductances at designed values, and which does not produce large distortion if input signal differential amplitude or DC component are larger than predetermined threshold voltages.

SUMMARY OF THE INVENTION

The invention has several salient advantages. For example, a transconductor is provided which controls the V_{GS} input such that the common-mode voltage of the current source transistors are maintained at a predetermined voltage in spite of manufacturing process variations.

Additionally, a transconductor is presented which maintains the ratio of transconductances at designed values.

Also, a transconductor is presented which does not produce large distortion if input signal differential amplitude or DC component are larger than predetermined threshold voltages.

These and other objects, features, and advantages of the invention will become apparent to those skilled in the art from the following detailed description, when read in conjunction with the accompanying drawing and appended claims.

According to a broad aspect of the invention, a transconductor is presented having first and second current flowpaths. Each of the current flowpaths has a current sourcing transistor, an input transistor, and a load transistor. The input transistors are connected to receive a differential input signal. A pair of transistors are provided, each connected to feed forward a signal between the input and the current sourcing transistors in a respective flowpath to a respective control element of the

load transistors. A resistor is connected between output nodes of the first and second flowpaths, and a current source, which may be adjustable, is connected between a common node of the load transistors and a reference potential. A voltage comparing amplifier is connected between the common node of the load transistors and control elements of the current sourcing transistors. The amplifier is referenced to a reference voltage, whereby a voltage on the common node controls current sourced by the current sourcing transistors. A plurality of differential load circuits are provided, each connected in parallel with the load transistors, and each including a controllable current source connected between a common node of the circuit and a reference potential. Additionally, a respective plurality of capacitive circuits each connected between the input transistor and the load transistor of each current flowpath may be provided.

According to another broad aspect of the invention, a method is presented for operating a transconductance circuit. The method includes controlling currents in first and second current flowpaths of the transconductance circuit to follow a common node voltage between the first and second flowpaths. The method also includes providing a plurality of differential pair load transistor circuits in parallel with differential load transistors in the flowpaths, each comprising a respective adjustable current source for adjustment of a transconductance of the transconductance circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated in the accompanying drawings, in which:

Figure 1 is an electrical schematic diagram of a transconductor circuit, in accordance with the prior art.

Figure 2 is an electrical schematic diagram of a transconductor circuit, in accordance with a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A transconductor is a voltage controlled differential transconductance stage, amplifier, or circuit. Transconductance circuits are used in many applications, among which, for example is in driver circuits that supply drive power to a dc motor used to spin a disk of a hard disk drive, or the like.

A transconductor 10, in accordance with a preferred embodiment of the invention, is shown in Figure 2. The transconductor 10 has a differential input signal applied to the gates of input transistors 12 and 14. PMOS current sourcing transistors 16 and 18 enable a feed forward voltage to be developed that is applied to differential load transistors 20 and 22 via transistors 24 and 26. Current sources 28 and 30 provide currents to the output transistor driving paths 25 and 27.

An adjustable or variable current source 34 is connected between the sources of the differential load transistors 20 and 22 and a reference potential, or ground. The current source 34 is adjustable as a part of the transconductance tuning, discussed below in detail.

A resistor 36 is connected between the source elements of transistors 12 and 14 on nodes 37 and 39 across which the differential output voltage is developed. The resistor 36 may be, for example, a MOSFET device that is sized and biased to operate in its triode or linear region. A plurality of transistor/capacitor circuits 40...42 and

44...46 are also connected to the sources, respectively, of transistors 12 and 14, as shown. The purpose of the switched transistor circuits 40, 42, 44, and 46 is to allow adjustment of LHP zero to reduce GDV (LHP = Left-Half Plane; GDV = Group Delay Variation).

More particularly, the presence of the capacitances at the source nodes of the differential load transistors 20 and 22 introduces LHP-zero. The bigger the total of the capacitances connected to these node pairs, the lower the frequency of this LHP-zero. Adjustment of this LHP-zero allows one degree of freedom in adjusting the frequency response of this transconductor to obtain a maximally flat group delay variation by adjusting the negative delay of the LHP-zero to partially cancel the positive delay of the poles within the loops formed by the transistors 20, 12, and 24, or by the transistors 22, 14, and 26.

A differential amplifier 38 is interconnected between the sources of load transistors 20 and 22 and the gates of the current source PMOS transistors 16 and 18. The differential amplifier 38 operates to compare the voltage on the sources of the output transistors 20 and 22 to a reference voltage V_B on its inverting input terminal, and forms part of the feedback loop that maintains the common source of transistors 20 and 22 at a desired voltage. Thus, if the common source of transistors 20 and 22 has a voltage departing from the voltage level of V_B , for instance, going higher, then the output of the amplifier 38 goes also higher. This, in turn, reduces the magnitude of $V_{gs}-V_{tp}$ of the PMOS devices 16 and 18, which results in less current being delivered into the drain nodes of transistors 12 and 14. As a result, the drain voltages of transistors 12 and 14 drop. As a consequence, through transistors 24 and 26,

level-shifting results, and the gate voltages of transistors 20 and 22 drop, which finally results in their common source voltage dropping to complete the desired negative feedback action. It should be noted that the amplifier 38 only needs to have low bandwidth since the fast differential signal does not propagate through it.

The reference voltage, V_B , applied to the amplifier 38 can be any desirable voltage, depending on the objective sought to be achieved by the circuit. For example, V_B can be a fixed voltage, for example, 300mV, in which case this common-mode feedback loop tries to maintain the common source of load transistors 20 and 22 at 300mV. On the other hand, V_B can be level-shifted down, for instance, by using two NMOS devices in series (in a manner similar to the series connection of the transistors 24 and 20) from a fixed voltage, say V_{CC} -400mV. In this case, the common-mode feedback loop tries to maintain the drain nodes of transistors 12 and 14 at a common-mode voltage of V_{CC} -400mV, which maximizes the common-mode input range. Alternatively, it could be level-shifted similarly, but from the common-mode voltage of the inputs themselves in order to guarantee that the drain voltages of transistors 12 and 14 are the same as the input common-mode voltage.

Additionally interconnected between the gates of the differential load transistors 20 and 22 to which the input signal is fed forward are a series of differential pair circuits 53, 61, and 63, each circuit including a transistor connected between input nodes 54 and 56 and a respective tunable current source. Thus, as shown, the first differential pair circuit includes transistors 50 and 52 connected between respective input nodes 54 and 56 and one side of a tunable current source 58. The current source

58 is controllable, and may be enabled or disabled, as desired. Similar circuit 61 and 63 are connected in parallel with the circuit 53.

The circuit 61 includes a transistor 62 connected between the input node 54 and a variable current source 64, and a transistor 66 is connected between the input node 56 and the variable current source 64. On the other hand, the circuit 63 includes a transistor 70, also connected between the input node 54 and a variable current source 72, as well as a transistor 74 that is connected between the input node 56 and the variable current source 72. Although three parallel circuits 53, 61, and 63 are shown, it should be understood that any number of circuits can be employed, using the current and sizing ratios discussed below.

Each of the parallel circuits 53, 61, and 63 contributes differential output current that is directly proportional to the current running through load transistors 20 and 22, and also directly proportional to the square root of the ratio between its own tail current (I_{t2} , for instance) and I_{t1} . It can be seen that the transconductance ratio between transistors 20-22 and 54-56,

for example, is $(R-1)\sqrt{\frac{I_{t2} + I_{t3} + \dots + I_{tn}}{I_{t1}}}$.

As mentioned above, the currents of each of the current sources 34, 58, 64, and 72 are individually controllable and individually enableable and disableable. This allows for a very wide transconductance tuning range in a piecewise continuous fashion. The transconductance ratio between transistors 20-22 and 54-56, as mentioned, is proportional to the square root of the quotient of the currents of current sources 34 and 58. On the other hand, the stepwise transconductance ratio is determined by the

ratio of the widths of the transistors of each respective transconductance determining stage. For example, the transconductance ratio determined by the ratio of the widths of transistors 20 and 54, which affects the stepwise transconductance ratio. For example, if four output differential pairs are used and the ratio of the sizes of the transistors 20, 50, 62, and 70 are 1:2:4:8, the currents of the current sources 34, 58, 68, and 72 enable a transconductance range of 16 to 1 to be enabled. (The transistors may be sized, for example, by laying out transistor gate widths in the ratios indicated, or other ratios, as desired.)

It should be noted that with the circuit 10 constructed as above described, the portions of the transconductor 10 that carry signals may be constructed entirely with NMOS devices, which increases the speed of the circuit, since NMOS devices, with higher carrier mobilities than comparable PMOS devices, are generally regarded as being four to five times faster than such PMOS devices.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.



CLAIMS:

1. A transconductor, comprising:

first and second current flowpaths each having a current sourcing transistor, an input transistor, and a load transistor, said input transistors being connected to receive a differential input signal;

a pair of transistors each connected to feed forward a signal between said input and said current sourcing transistors in a respective flowpath to a respective control element of said load transistors;

a resistor connected between output nodes of said first and second flowpaths;

a current source connected between a common node of said load transistors and a reference potential;

and a voltage comparing amplifier connected between said common node of said load transistors and control elements of said current sourcing transistors, said amplifier being referenced to a reference voltage, whereby current sourced by said current sourcing transistors is controlled by a voltage on said common node.

2. The transconductor of claim 1 wherein said current source connected to said common node is adjustable, and further comprising a plurality of differential load circuits, each circuit being connected in parallel with said load transistors, and each circuit including a controllable current source connected between a common node of said circuit and a reference potential.

3. The transconductor of claim 2 wherein respective ones of said load transistors and respective load transistors of said load circuits are sized with ratios of 1:2:4:8.



4. The transconductor of claim 1 further comprising a respective plurality of capacitive circuits each connected between said input transistor and said load transistor of each current flowpath.

5. The transconductor of claim 4 wherein said capacitive circuits each comprise a capacitor and a switching transistor for controllably connecting said capacitor between said input transistor and said load transistor.

6. The transconductor of claim 1 wherein said input transistor, said load transistor, and said feed forward transistors are NMOS transistors.

7. The transconductor of claim 1 wherein said resistor is a MOS transistor biased to operate in a linear mode.

8. A transconductor, comprising:

first and second current flowpaths each having a current sourcing transistor, an input transistor, and a load transistor, said input transistors being connected to receive a differential input signal;

a pair of transistors each connected to feed forward a signal between said input and said current sourcing transistors in a respective flowpath to a respective control element of said load transistors;

a resistor connected between output nodes of said first and second flowpaths;

an adjustable current source connected between a common node of said load transistors and a reference potential; and



a plurality of differential load circuits, each circuit being connected in parallel with said load transistors, and each circuit including a controllable current source connected between a common node of said circuit and a reference potential.

9. The transconductor of claim 8 wherein respective ones of said load transistors and respective load transistors of said load circuits are sized with ratios of 1:2:4:8.

10. The transconductor of claim 8 further comprising a voltage comparing amplifier connected between said common node of said load transistors and control elements of said current sourcing transistors, said amplifier being referenced to a reference voltage, whereby current sourced by said current sourcing transistors is controlled by a voltage on said common node.

11. The transconductor of claim 8 further comprising a respective plurality of capacitive circuits each connected between said input transistor and said load transistor of each current flowpath.

12. The transconductor of claim 11 wherein said capacitive circuits each comprise a capacitor and a switching transistor for controllably connecting said capacitor between said input transistor and said load transistor.

13. The transconductor of claim 8 wherein said input transistor, said load transistor, said feed forward transistors, and transistors of said differential load circuits are NMOS transistors.



14. The transconductor of claim 8 wherein said resistor is a MOS transistor biased to operate in a linear mode.

15. A method for operating a transconductance circuit, comprising:

controlling currents in first and second current flowpaths of said transconductance circuit to follow a common node voltage between said first and second flowpaths;

and providing a plurality of differential pair load transistor circuits in parallel with differential load transistors in said flowpaths, each comprising a respective adjustable current source for adjustment of a transconductance of said transconductance circuit.

16. The method of claim 15 wherein said controlling currents in first and second current flowpaths of said transconductance circuit to follow a common node voltage between said first and second flowpaths comprises comparing a voltage on said common node to a reference voltage, and adjusting a supply current to said flowpaths according to said comparing.

17. The method of claim 15 further comprising sizing transistors of said differential pair load transistor circuits and said differential load transistors in said flowpath to have a size ratio of 1:2:4:8.

18. The method of claim 15 further comprising adjusting said adjustable current sources to control a transconductance of said transconductance circuit.



19. The method of claim 17 further comprising adjusting said adjustable current sources to control a transconductance of said transconductance circuit.

20. The method of claim 15 further comprising connecting a respective plurality of capacitive circuits between said input transistor and said load transistor of each current flowpath.