Title of the Invention

Substrate level 3D Package for Semiconductor Devices

Field of the Invention

This invention relates to a method of making a small form factor 3 Dimensional package using a multiplicity of silicon chips arranged in vertical stack format. In particular, the method provides a combination of active silicon chips mounted on a flex or rigid substrates and interconnected vertically to achieve increased functionality and reduced foot print on the mother boards. The package produced in this method utilizes single chip foot print.

Background of the Invention

The conventional practice of silicon device / component assembly on circuit boards is to assemble the individually packaged semiconductor components using SMT lines. The circuit boards are fairly larger in size for these component assemblies due to the thick population of components including discrete devices such as resistors, capacitors and inductors. These practices were very well accepted in the past may be a decade ago, as the systems that were manufactured were fairly larger in size. We could assemble many components, even multiple numbers of same components to obtain more functionality such as memory and so on on the same board and meet the consumer requirements.

However, In the recent past the consumer market is driven by miniaturized products due to portability, lower costs, and other numerous requirements by the consumers. Large sized products are no more accepted and hence there became a need for developing miniature sized products to meet the consumer market. Number of semiconductor industry including design houses, fab houses are continuously shrinking the device feature sizes and adding more and more functionality in single chips in the form of System on Chip (SOC), System in Package (SIP) and so on. At the same time packaging industry are also being driven by miniaturized packages with increased functionality per package.

This invention approach is expected to meet such a requirement of miniaturized product, as it offers increased functionality combined with reduced cost at very small foot prints on the circuit boards. For example, in a computer system, under current practice, a 128 MB memory will require a board arrea of about 12 cm X 12 cm square. This method of invention will require as much as 2 cm square area for the same 128 MB memory. Here in this method 8 single memory chips of 16 MB are stacked vertically and still arrive at 128 MB memory capacity. We can stack multiple functional devices together and achieve functions similar to SOC / SIP integrations.

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Brief Description of Prior art

Currently a number of 3 Dimensional packages have been developed by many Japanese semiconductor houses. Few of these are briefly described as follows:

1. Two Die Stack package:
   This method uses two die. One a small die and other a larger die.
   A larger chip is die attached on a pre-fabricated substrate. A smaller chip is die attached directly above the larger die. Wire bonding performed from both larger and smaller dies to the common substrate. The dies above the substrate are molded. This two die package is then surface mounted (Fig. 12).

2. Three Die Stack Package:
   This method uses three die. One a small die, the second a larger die and the third a much larger die. The stack package is that of similar process to above described two die stack package (Fig. 13)

3. Wafer Level Stack Package:
   This method uses stacking of wafers vertically by through hole etch and metal filling to interconnect all the I/O's vertically. The wafers are need to be precisely aligned and wafer bonded using sophisticated and expensive front end fab equipment (Fig. 14)

Summary of the Invention

In accordance with the Invention, a new three dimensional package has been designed for Fabrication as follows. For simple functionality test purposes, a daisy chain test chip to be used for package fabrication. A substrate (organic / ceramic) is pre – fabricated with a similar pad patterns on both sides. The metal patterns on both sides are shorted using a hole that is deposited with metal. The pad patterns are designed as per the stacked chip configuration. The substrate could be in strip form, or panel form depending on assembly house capability. Silicon dies are die attached on the substrate and wirebonded as per wirebond diagram. The substrate with assembled dies are molded and cured. Suitable processes are carried out on the front side of the substrate to expose wire loops. These exposed wire loops are interconnected with substrate bottom patterns by proper alignment, thus stacking the substrates vertically. The number of substrate layers in a stack can be determined by the functionality of the product in consideration. The stacked substrates / assembly are then diced and each stack module is separated.

The IC stack modules are then surface mounted on the mother / circuit boards.

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Brief Description of Drawings

The benefits, nature and various features of the invention are to appear fully upon consideration of the illustrative embodiments to be described in detail in connection with the accompanying drawings. In the drawings:

Fig. 1 shows a general functional wafer showing individual chips separated by scribe lines.

Fig. 2 shows a substrate layout showing patterns that are corresponding to wire bond interconnect fingers on the substrate (Flex / Rigid).

Fig. 3 shows a cross section of a substrate and die after die attachment is carried out.

Fig. 4 shows a cross section of a substrate and die after die attach and wire bonding performed.

Fig. 5 shows a cross section of a substrate and die after die attach, wire bond and molding process performed.

Fig. 6 shows a cross section of a substrate and die after die attach, wire bond, molding and grinding on the front side to expose the wire leads.

Fig. 7 shows a metal deposition and patterning on top of the wire loops above the molded Substrate.

Fig. 8 shows a deposited solder material directly on top of the patterned metal over the wire loop.

Fig. 9 shows a vertical stack assembly process step using two individual chip assemblies by placing one on top of the other after alignment.

Fig. 10 shows a vertical stack assembly process after number of individual chip assemblies are stacked one on top of the other and reflown.

Fig. 11 shows a completely encapsulated stack package using a suitable molding process.

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Detailed Description of the Invention:

Embodiment for the Invention:

Referring to the drawings, Fig. 1 is a schematic diagram of a standard wafer with number of functional die arrayed and separated by a scribe line. This method of Invention can be used for 3D packaging of any silicon die that can be packaged on a substrate using wire bond process. Fig. 2 is a schematic diagram of a cross section of a Flex substrates (Organic / Ceramic) with predetermined sizes. The patterns are defined based on chip bond pad configuration and pad pitch. Metal Patterns are etched on both the sides of the flex substrate as per good solder interconnect requirement. NiAu thin film is required for exposed metal patterns from preventing the metal film from oxidization. Fig. 3 is a schematic diagram of a known good die (KGD) (1) that has been die attached on a substrate.

Fig. 4 is a schematic diagram of the wire bonded (2) between die (1) and substrate (Fig. 2). It is ensured that uniform wire bond loops are obtained in wire bond process. Fig. 5 is a schematic diagram of a substrate and die assembly that has been molded using a polymeric material (3) on front top side of the substrate directly above the silicon die (1) with wire bond (2) loops. The polymeric material (3) can be molded using a transfer molding process or screen printing method using special screen print machine / stencils. Fig. 6 is a schematic diagram detailing a cross section after grinding process on the front side of the substrate directly over the polymeric layer. Grinding process is carried out to expose the Gold /Aluminium / Cu wire loops (4) directly above the molded substrate.

Fig. 7 is a schematic diagram showing the exposed wire loop (4) which are deposited with a suitable solder wetting thin film (5). Atleast 5 micron thickness of the thin film is required for obtaining a good interconnection. Fig. 8 is a schematic diagram showing substrate processed above and are solder coated (6) directly on the deposited solder wetting pads (Fig. 8). The solder coating process can be any of the current solder deposition methods available in the market. Also the solder types can be any commonly used solders including high lead and lead free solders. Fig. 9 is a schematic diagram showing alignment of substrate assembly with corresponding top pad locations of the package to the bottom pad locations of the substrate (7) assembly in stacked manner and reflown to interconnect vertically. Fig. 10 is a schematic diagram of multiple chips stacked vertically to make a high density 3 Dimensional package (8) to achieve high functionality with reduced foot print. Fig. 11 is a schematic diagram of the above stack package after the same has been molded (9) to arrive at a single 3D packaged substrate. Further dicing process is used to separate each 3D module with multiple chip assembled in it. The individual 3D modules are assembled to mother boards using SMT line. This method of invention also allows solder bumping of the exposed pads at the bottom of the package in substrate form or in individual module form.

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CLAIMS:

1. A method for making a 3 Dimensional integrated circuit package that provides a high density function combined with reduced foot print and low cost have been discussed.

2. The method of invention at 1 above claims fabrication of a substrate with identical conductive thin film patterns on the both sides of the substrate.

3. The method of invention at 1 above claims the substrate be made of organic or ceramic base laminate.

4. The method of invention at 1 above claims the conductive thin film patterns be etched / printed / laminated thin films of conductive nature.

5. The method of invention at 1 above claims the top and bottom thin film patterns on the substrate are connected by through hole connection methods.

6. The method of invention at 1 above claims the through holes be either conductive plated or conductor metal filled.

7. The method of invention at 1 above claims use of wafer thickness more than or equal to 30 micron.

8. The method of invention at 1 above claims standard die bond and wire bonding process.

9. The method of invention at 1 above claims the use of conductive / non conductive die attach polymers / epoxies.

10. The method of invention at 1 above claims the wire bonds be made of Aluminium / Gold / Copper wires of diameter greater than 0.8 mil.

11. The method of invention at 1 above claims semiconductor grade non conductive polymeric epoxies that are suitable for molding process.

12. The method of invention at 1 above claims the molding process be transfer molded or screen printed methods.

13. The method of invention at 1 above claims grinding / any form of etching of molded polymer on the front side of the assembly to expose wire loops.

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14. The method of invention at 1 above claims the wire loop area be enlarged by most commonly available conductive metal deposition methods.

15. The method of invention at 1 above claims the deposition methods be sputter / plated / evaporated thin films.

16. The method of invention at 1 above claims the deposited thin films be solder wetting in property.

17. The method of invention at 1 above claims solder deposition at the enlarged wire loop pad locations.

18. The method of invention at 1 above claims the solder deposition methods be standard methods practiced in SMT assembly lines including wave soldering and Hot Air Leveling methods.

19. The method of invention at 1 above claims stacking of substrates by alignment of corresponding top and bottom solder deposited pads and reflow.

20. The method of invention at 1 above claims stacking of individual die assemblies after dicing and separating single die assemblies.

21. The method of invention at 1 above claims stack package for different functional chips by way of appropriate substrate patterning and interconnections.

22. The method of invention at 1 above claims over molding of the entire stack package after the stack assembly done.

23. The method of invention at 1 above claims assembly of each stack module to mother board using SMT line.

24. The method of invention at 1 above claims solder bumping on the bottom substrate pads as per conventional printing methods.

25. The method of invention at 1 above claims easy testing of individual stack modules before the final assembly on mother boards.

26. The method of invention at 1 above claims foot print that is equal to single chip / substrate assembly.



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