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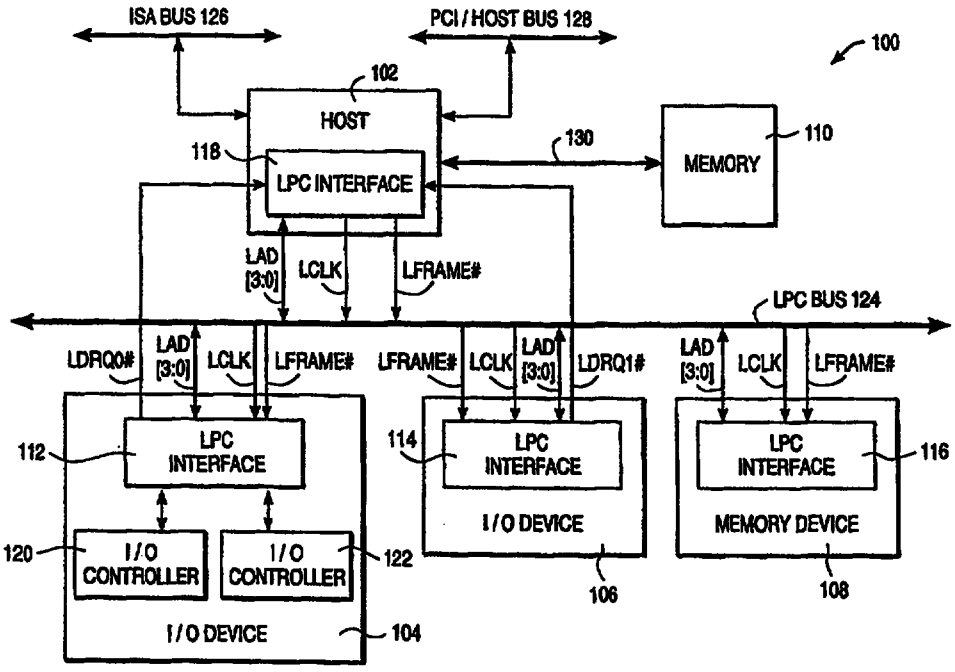
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(54) Title: DIRECT MEMORY ACCESS (DMA) TRANSACTIONS ON A LOW PIN COUNT BUS



(57) Abstract

A system including a host (102) coupled to a memory device (108) and a peripheral controller device (120). The host (102) is coupled to the peripheral controller device (120) via bus (124) having a plurality of general purpose signal lines to carry time-multiplexed address, data, and control information. The peripheral controller device (120) performs a direct memory access (DMA) transactions with the memory device (108) via the host (102) the bus (124).