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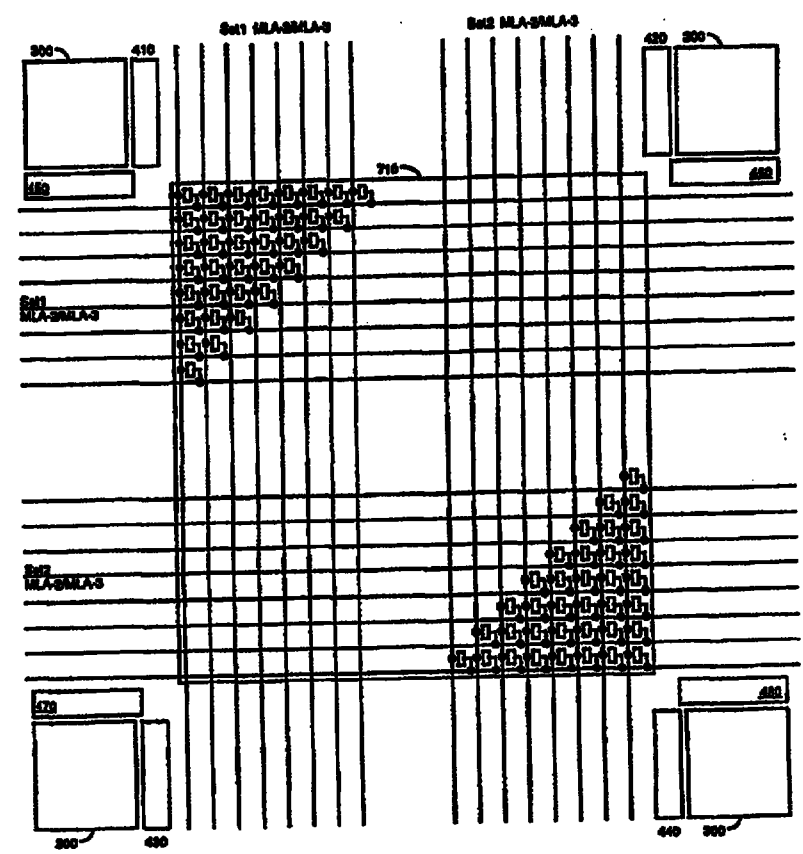
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(54) Title: SCALABLE MULTIPLE LEVEL INTERCONNECT ARCHITECTURE

(57) Abstract

An improved field programmable gate array (FPGA) is provided which includes tab network connectors (410, 420, 430 ... 470) for interfacing groups of configurable function generators with lower levels of interconnect and for interfacing lower levels of interconnect with higher levels of interconnect. Furthermore, an innovative cluster architecture is utilized which provides fine granularity without a significant increase in configurable function generators. The tab connector network (410, 420 ... 470) can also be used to route a lower level routing line to a higher level routing line. This is particularly desirable in order to meet the needs for driving a signal along longer routing lines without requiring all signal drivers be sufficiently large to drive a signal along the longest routing line. The connector networks described enable a flexible routing scheme to be implemented in which the routing lines at each level are divided into sets. In addition, the innovative routing hierarchy consisting of the routing lines, block connector tab networks and turn matrices (710), permits an innovative, space saving floor plan to be utilized that is scalable.



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