CLAIMS

1. A method for forming a semiconductor structure, comprising:

providing a semiconductor substrate, wherein stack structures and isolation structures alternately arranged along a first direction are formed on the semiconductor substrate;

forming a support structure in the stack structures and the isolation structures;

etching the stack structures and the isolation structures to form a plurality of zigzag first semiconductor pillars in an array arrangement along the first direction and a second direction, wherein an interspace is formed between the zigzag first semiconductor pillars; each of the zigzag first semiconductor pillars comprises first convex structures and first concave structures alternately arranged along a third direction, and the zigzag first semiconductor pillars are supported by the support structure; the first direction, the second direction and the third direction are perpendicular to one another, and the second direction is perpendicular to a top surface of the semiconductor substrate; and

forming capacitor structures the interspace.

2. The method according to claim 1, wherein each of the stack structures comprises first semiconductor layers and second semiconductor layers alternately stacked along the second direction; and the zigzag first semiconductor pillars are formed by:

forming a mask layer with a specific pattern on surfaces of the stack structures and the isolation structures, wherein the specific pattern comprises a plurality of sub-patterns arranged along the third direction in sequence, and the sub-patterns exposes part of each of the stack structures and part of each of the isolation structures; and

forming the first concave structures by thinning each of the second semiconductor layers in each of the stack structures exposed by the sub-patterns; wherein an untreated part of each of the second semiconductor layers constitutes the first convex structures; and a projection area

of each of the first convex structures along the third direction is greater than a projection area of each of the first concave structures along the third direction.

3. The method according to claim 2, wherein before forming the first concave structures, the method further comprises:

removing the isolation structures exposed by the sub-patterns and the first semiconductor layers of the stack structures exposed by the sub-patterns by using the mask layer.

4. The method according to claim 3, wherein after forming the first concave structures, the method further comprises:

removing the mask layer, the remaining first semiconductor layers and the remaining isolation structures in sequence.

5. The method according to claim 2, wherein the stack structures and the isolation structures are formed by:

forming an initial stack structure on the semiconductor substrate, wherein the initial stack structure comprises the first semiconductor layers and the second semiconductor layers alternately stacked;

patterning the initial stack structure to form the stack structures and isolation trenches; and

filling an isolation material in the isolation trenches to form the isolation structures.

6. The method according to claim 5, wherein patterning the initial stack structure to form the

stack structures and the isolation trenches comprises:

forming a first mask layer having a first preset pattern on a surface of the initial stack structure, wherein the first preset pattern comprises a plurality of first preset sub-patterns arranged along the first direction in sequence and the first preset pattern exposes part of the initial stack structure; and

etching the initial stack structure by the first mask layer to remove the initial stack structure exposed by the first preset sub-patterns, to form the stack structures and the isolation trenches.

7. The method according to any one of claims 2 to 6, wherein forming the support structure in the stack structures and the isolation structures comprises:

forming a second mask layer having a second preset pattern on the surfaces of the stack structures and the isolation structures, wherein the second preset pattern exposes part of each of the stack structures and part of each of the isolation structures;

removing the exposed isolation structures and the second semiconductor layers of the exposed stack structures by the second mask layer by etching to form etching grooves; and

filling a support material in the etching grooves to form the support structure.

8. The method according to claim 1, wherein forming the capacitor structures in the interspace comprises:

forming a first electrode layer, a dielectric layer and a second electrode layer on a surface of each of the zigzag first semiconductor pillars to form the capacitor structures.

9. The method according to claim 8, wherein the method further comprises:

filling a conducting material in an interspace between the second electrode layers to form a conducting layer.

10. The method according to claim 4, wherein after forming the first concave structures and before removing the mask layer, the remaining first semiconductor layers and the remaining isolation structures in sequence, the method further comprises:

rounding the first concave structures to form first cylinders.

11. The method according to claim 10, wherein after removing the mask layer, the remaining first semiconductor layers and the remaining isolation structures in sequence, the method further comprises:

rounding the first convex structure to form second cylinders, wherein the first cylinders and the second cylinders together constitute the zigzag second semiconductor pillars.

12. The method according to claim 11, wherein the method further comprises:

forming the capacitor structures in the interspace between zigzag second semiconductor pillars to form the semiconductor structure.

13. The method according to claim 8, wherein the method further comprises:

performing ion implantation on the zigzag first semiconductor pillars.

14. The method according to claim 12, wherein the method further comprises:

performing ion implantation on the zigzag second semiconductor pillars.

15. The method according to claim 13, wherein the method further comprises:

forming a metal silicide on surfaces of the zigzag first semiconductor pillars.

16. The method according to claim 14, wherein the method further comprises:

forming a metal silicide on surfaces of the zigzag second semiconductor pillars.

17. A semiconductor structure comprising:

a semiconductor substrate;

a plurality of zigzag first semiconductor pillars and a support structure located on a surface of the semiconductor substrate; wherein the plurality of the zigzag first semiconductor pillars are in an array arrangement along a first direction and a second direction and are supported by the support structure; each of the zigzag first semiconductor pillar comprises first convex structures and first concave structures alternately arranged along a third direction in sequence; and the first direction, the second direction and the third direction are perpendicular to one another, and the second direction is perpendicular to a plane where the semiconductor substrate is located; and

capacitor structures filled between the zigzag first semiconductor pillars.

18. The structure according to claim 17, wherein a projection area of each of the first convex structures on the third direction is greater than a projection area of each of the first concave structure on the third direction.

19. The structure according to claim 17 or 18, wherein each of the capacitor structures comprises a first electrode layer, a dielectric layer and a second electrode layer; and the

semiconductor structure further comprises a conducting layer; and

the conducting layer is filled between second electrode layers.