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METHODS OF ELECTROPLATING SOLDER BUMPS OF UNIFORM HEIGHT ON INTEGRATED CIRCUIT SUBSTRATES

Abstract of the Disclosure

Methods of electroplating solder bumps of uniform height on integrated circuit substrates include the steps of drawing plating current through an integrated circuit wafer by electrically shorting an integrated circuit's ground, power and signal pads together using an ultra-thin plating base layer (e.g., < 0.075μm thick) and then using a backside wafer contact to draw electroplating current along parallel paths which extend through the ground and signal pads and into the substrate. The ground pads are preferably electrically coupled to the substrate at substrate contact regions (e.g., N+ or P+ diffusion regions) and the signal pads are preferably electrically coupled to the substrate through active semiconductor devices (e.g., FETs, BJTs, ...) to which the signal pads are attached. Plating current is preferably drawn in parallel through an integrated circuit's active semiconductor devices and substrate contact regions. The combined contributions of the plating currents drawn through the substrate contact regions and the active semiconductor devices is sufficient to maintain the plating base layer and underlying pads at uniform potentials even though the plating base layer has a preferred thickness of less than about 0.075μm. These uniform and typically non-zero potentials cause the rates of electroplating to be highly uniform across the wafer by limiting lateral current flow through the plating base layer. The uniformity of the electroplated solder bumps can also be enhanced by using high density controlled collapse chip connection (C4) ("flip-chip") technologies and by interspersing the ground and signal pads on each "flip-chip" so that each signal pad has at least one ground pad as a nearest neighbor.

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