

ABSTRACT

An internal error-checking circuit includes a clock generation circuit, an internal command generation circuit, an address generation circuit, a control logic circuit, and an error correction circuit. The clock generation circuit generates and outputs a self-refresh clock
5 signal in response to a self-refresh enable signal; the internal command generation circuit counts the self-refresh clock signals when the error-checking enable signal indicates that an internal error-checking function is enabled and generates and outputs one internal error-checking command signal when the count value of the self-refresh clock signal is a first preset value; the address generation circuit counts the internal error-checking command signal to
10 generate and output an internal error-checking address; the control logic circuit controls, in response to the internal error-checking command signal, the error correction circuit to sequentially execute a single internal read-modify-write operation on the target memory cells corresponding to the internal error-checking address in a plurality of memory arrays.

[FIG. 1]