(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 May 2005 (26.05.2005)

PCT

(10) International Publication Number
WO 2005/048320 A3

(51) International Patent Classification[7]: H01L 21/8238

(21) International Application Number:
PCT/US2004/028486

(22) International Filing Date: 31 August 2004 (31.08.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/654,689 4 September 2003 (04.09.2003) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

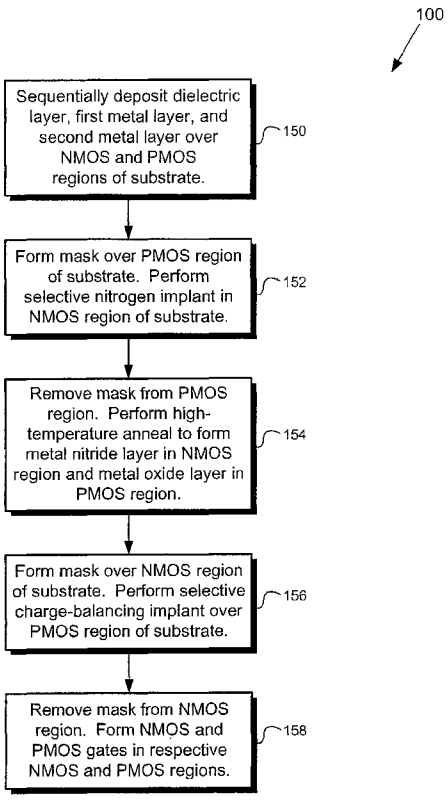
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **XIANG, Qi** [CN/US]; 1119 Thames Drive, San Jose, CA 95129 (US). **ZHONG, Huicai** [CN/US]; 509 Popula Blvd., Wappingers Falls, NY 12509 (US). **GOO, Jung-Suk** [KR/US]; 100 Escondido Village, #D, Stanford, CA 94305 (US). **HOLBROOK, Allison, Kay** [US/US]; 21187 Almaden Road, San Jose, CA 95120 (US). **JEON, Joong, S.** [US/US]; 10705 Flora Vista Avenue, Cupertino, CA 95014 (US). **KLUTH, George, Jonathan** [US/US]; 112 Heritage Village Way, Campbell, CA 95008 (US).

(74) Agent: **COLLOPY, Daniel, R.**; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

[Continued on next page]

(54) Title: METHOD FOR INTEGRATING METALS HAVING DIFFERENT WORK FUNCTIONS TO FORM CMOS GATES HAVING A HIGH-K GATE DIELECTRIC AND RELATED STRUCTURE



(57) Abstract: According to one exemplary embodiment, a method for integrating first (206) and second metal layers (208) on a substrate (202) to form a dual metal NMOS gate (226) and PMOS gate (228) comprises depositing (150) a dielectric layer (204) over an NMOS region (210) and a PMOS region (212) of the substrate (202). The method further comprises depositing (150) the first metal layer (206) over dielectric layer (204). The method further comprises depositing (150) the second metal layer (208) over the first metal layer (206). The method further comprises implanting (152) nitrogen in the NMOS region (210) of substrate (202) and converting (154) a first portion of the first metal layer (206) into a metal oxide layer (220) and converting a second portion of the first metal layer (206) into metal nitride layer (218). The method further comprises forming (156) the NMOS gate (226) and the PMOS gate (228), where the NMOS gate (226) comprises a segment (234) of metal nitride layer (218) and the PMOS gate (228) comprises a segment (242) of the metal oxide layer (220).

WO 2005/048320 A3

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) **Date of publication of the international search report:**
27 October 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.