CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a substrate which includes a cell region and a core region;

a boundary element separation film which is placed inside the substrate, and separates the cell region and the core region;

a bit line which is placed on the cell region and the boundary element separation film and extends along a first direction; and

a bit line capping film which extends along the first direction, on the bit line;

wherein the boundary element separation film includes a first region and a second region,

a height of an upper side of the first region of the boundary element separation film is different from a height of an upper side of the second region of the boundary element separation film, on a basis of a bottom side of the boundary element separation film,

the bit line is placed over the first region of the boundary element separation film and the second region of the boundary element separation film, and

a thickness of the bit line capping film in the first region of the boundary element separation film is smaller than a thickness of the bit line capping film in the second region of the boundary element separation film.

2. The semiconductor device of claim 1, wherein the first region of the boundary element separation film is nearer to the cell region than the second region of the boundary element separation film, and

the height of the upper side of the first region of the boundary element separation film is higher than the height of the upper side of the second region of the boundary element separation film.

3. The semiconductor device of claim 1 or claim 2, wherein the boundary element separation film further includes a third region,

the second region of the boundary element separation film is placed between the first region of the boundary element separation film and the third region of the boundary element separation film, and

a height of an upper side of the third region of the boundary element separation film is higher than the height of the upper side of the second region of the boundary element separation film, on the basis of the bottom side of the boundary element separation film.

4. The semiconductor device of claim 1 or claim 2, wherein the core region of the substrate is immediately adjacent to the second region of the boundary element separation film.

5. The semiconductor device of any one of claims 1 to 3, further comprising:

a separation region capping film which is placed on the second region of the boundary element separation film,

wherein the separation region capping film does not extend to the first region of the boundary element separation film.

6. The semiconductor device of claim 1, wherein an upper side of the bit line capping film in the first region and an upper side of the bit line capping film in the second region are placed on a same plane.

7. The semiconductor device of any one of claims 1 to 3, further comprising:

a buffer layer extending along the first direction, below the bit line,

wherein on the boundary element separation film, the buffer layer extends along profiles of the upper side of the first region and the upper side of the second region of the boundary element separation film.

8. A semiconductor device comprising:

a substrate which includes a cell region and a core region;

a boundary element separation film which is placed inside the substrate, and separates the cell region and the core region;

a separation region capping film which is placed on the boundary element separation film; and

a bit line which is placed on the cell region and the boundary element separation film and extends along a first direction,

wherein the boundary element separation film includes a first region, a second region and a third region,

the second region of the boundary element separation film is placed between the first region of the boundary element separation film and the third region of the boundary element separation film,

the separation region capping film is placed on the second region of the boundary element separation film, and is not placed on the first region of the boundary element separation film and the third region of the boundary element separation film,

an upper side of the first region of the boundary element separation film and an upper side of the third region of the boundary element separation film are placed on a plane the same as that of an upper side of the separation region capping film, and

the bit line is placed over the first region of the boundary element separation film and the second region of the boundary element separation film.

9. The semiconductor device of claim 8, wherein the first region of the boundary element separation film is nearer to the cell region than the second region of the boundary element separation film.

10. The semiconductor device of claim 8 or claim 9, wherein a height of the upper side of the first region and the upper side of the third region of the boundary element separation film is higher than a height of an upper side of the second region of the boundary element separation film.

11. The semiconductor device of any one of claims 8 to 10, further comprising:

a buffer layer extending along the first direction, below the bit line,

wherein on the boundary element separation film, the buffer layer extends along profiles of the upper side of the first region of the boundary element separation film and the upper side of the separation region capping film on the second region.

12. The semiconductor device of any one of claims 8 to 11, further comprising:

a bit line capping film which extends along the first direction on the bit line, and is placed over the first region of the boundary element separation film and the second region of the boundary element separation film,

wherein an upper side of the bit line capping film on the first region and an upper side of the bit line capping film on the second region are located on a same plane.

13. A semiconductor device comprising:

a substrate which includes a cell region and a core region;

a boundary element separation film which is placed inside the substrate, separates the cell region and the core region, and includes a first region and a second region;

a bit line structure which is placed on the cell region and the boundary element separation film, and includes a bit line extending along a first direction and a bit line capping film placed on the bit line;

a gate electrode which is placed inside the substrate of the cell region and intersects the bit line; and

a buffer layer which is placed on the boundary element separation film and extends along the first direction,

wherein the bit line is placed over the first region of the boundary element separation film and the second region of the boundary element separation film,

the buffer layer is placed between the boundary element separation film and the bit line on the first region of the boundary element separation film, and is not placed on the second region of the boundary element separation film, and

a lower side of the bit line comes into contact with an upper side of the buffer layer in the first region and comes into contact with an upper side of the boundary element separation film in the second region.

14. The semiconductor device of claim 13, wherein a height of an upper side of the first region of the boundary element separation film is different from a height of an upper side of the second region of the boundary element separation film, on a basis of a bottom side of the boundary element separation film.

15. The semiconductor device of claim 13 or claim 14, wherein the bit line capping film extends along the first direction on the bit line, and

a thickness of the bit line capping film in the first region of the boundary element separation film is smaller than a thickness of the bit line capping film in the second region of the boundary element separation film.

16. The semiconductor device of claim 15, wherein an upper side of the bit line capping film in the first region and an upper side of the bit line capping film in the second region are placed on a same plane.

17. The semiconductor device of any one of claims 13 to 16, wherein the first region of the boundary element separation film is nearer to the cell region than the second region of the boundary element separation film.

18. The semiconductor device of claim 13, wherein the boundary element separation film further includes a third region,

the second region of the boundary element separation film is placed between the first region of the boundary element separation film and the third region of the boundary element separation film, and

a height of an upper side of the third region of the boundary element separation film is higher than a height of an upper side of the second region of the boundary element separation film.

19. The semiconductor device of any one of claims 13 to 17, wherein the core region of the substrate is immediately adjacent to the second region of the boundary element separation film.