

HIGH-SPEED PACKET SWITCH

Abstract

A packet switch of the type in which packets received in the switch are stored in memory until they are output. In the switch fabric of the switch, packets are serially
5 received in input shift registers (401) wide enough to store an entire packet, output in parallel to memory (407) which is as wide as the input shift register, moved in parallel in the memory, and output in parallel to an output shift register (405). The bus (403) connecting the input shift registers, the output shift register, and the memory is as wide as the input shift register, but does not cross the boundaries of the
10 semiconductor chips making up the switch fabric, thus avoiding the electrical problems of very wide buses. In the disclosed implementation, there are 14 input lines and 14 output lines. A switch memory is associated with each output line and receives packets from all 14 input lines, accepting only those destined for the output line associated with the input line. Each switch memory includes a controller,
15 memory and a communications interface for the controller, and a set of switch memory VLSI devices. Each switch memory VLSI device includes a first shift register for receiving slices of the packet and a bus, a memory, and a second shift register for outputting the slices. The bus, the memory, and the second shift register are as wide as the first shift register.

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This Sheet Has Been Replaced

