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"A SEMICONDUCTOR MEMORY DEVICE".

The present invention relates to a semiconductor memory device, and particularly to an art that can be effectively adapted to semiconductor memory devices of a highly integrated form.

A semiconductor memory device has memory cell arrays in which a plurality of memory cells are arranged in the form of a matrix on a semiconductor chip. In memory cell arrays are formed a plurality of word lines that extend in one direction. On the word lines are formed a plurality of data lines with an intermediate insulating film therebetween, the data lines extending in a direction at right angles with the word lines.

Accompanying the progress toward a high degree of integration, word lines and data lines have become finer. For instance, in a dynamic RAM (random access memory) of 256 K bits, the pattern width is about 2μm.

However, the yield decreases as the patterns become finer. Therefore, a so-called redundancy configuration has been employed to replace a fail or a malfunctioning bit, row or column with a spare element.

According to research which we have carried out, the portions that are replaced most frequently are word lines at the ends of the memory cell arrays. We attribute the cause to the following reasons.

The word lines are coated with an intermediate insulating film consisting of a phosphosilicate glass or the like, and data lines are formed thereon. Contact holes are formed in the intermediate insulating film prior to forming the data lines.

The thickness of a resist film for forming the contact holes is limited to, for example, about 1 μm from the standpoint of precision for forming patterns of contact holes. Since the resist film is in a fluid state such processing as spin coating and backing, the resist film thickness is less on protruded portions than in recessed portions. Therefore, the resist film is thinner on the word lines formed on the electrode layers of capacitors formed on a thick field oxide film than on other portions.

In particular, the resist film is thinnest at portions of word lines located at the ends of memory cell arrays. Since no word line exists on one side of these word lines, it is considered that the resist film tends to flow toward the direction where no word line exists. The thickness of the resist film varies depending upon the underlying pattern.

To form fine contact holes, dry etching is employed. Further, over-etching is perfomred so that the surface of the substrate is completely exposed.

The resist film is etched during dry etching by several thousands of angstroms overall. In the portions where the resist film is thin, in particular, the resist film is removed and the underlying intermediate insulating film is exposed. The intermediate insulating film which is exposed is easily etched. Therefore, the word lines under the intermediate insulating film are subjected to etching, causing defects such as line breakage.

Word line breakage develops locally in the portions where the resist film is particularly thin.

This defect develops not only in the word lines at the ends of the memory cell arrays but also in the dummy cell-selecting word lines in the dummy cell arrays.

It is an object of the present invention to provide a technique which effectively solves the problem associated with the processing of resist in producing semiconductor memory devices of a highly integrated form.

Another object of the present invention is to prevent the word lines from breaking in the semiconductor memory devices of a highly integrated form.

According to one aspect of the present invention there is provided a semiconductor memory device including:

(a) memory cell arrays including a plurality of memory cells that are formed in rows and in columns on a semiconductor substrate;

(b) a plurality of data lines comprised of an aluminium layer, said data lines being formed in columns and coupled to said memory cells that are arrayed in corresponding columns;

(c) a plurality of word lines comprised of polycrystalline silicon and a molybdenum silicide, said word lines being formed in rows and

coupled to said memory cells that are arrayed in corresponding rows; and

(d) wiring which is formed on the outside of, and adjacent to, said plurality of word lines formed in rows, said wiring extending in the same direction as said word lines, being composed of the same material as said word lines, and being formed simultaneously with the formation of the word lines.

According to a second aspect of the present invention there is provided a semiconductor memory device including:

(a) memory cell arrays including a plurality of memory cells that are formed in rows and in columns on a semiconductor substrate, each of said memory cells including a first capacitor for storing an electric charge, and a first MISFET connected in series therewith;

(b) dummy cell arrays including a plurality of dummy cells that are formed on the semiconductor substrate and that generate a reference level, each of said dummy cells including a second capacitor for storing an electric charge, a second MISFET connected in series therewith, and a third MISFET for discharging the electric charge stored therein into said second capacitor;

(c) a plurality of data lines formed in

columns, said data lines being coupled to said first MISFET's and said second MISFET's that are arrayed in corresponding columns;

(d) a plurality of word lines formed in rows, said word lines being coupled to said first MISFET's and said second MISFET's that are arrayed in corresponding rows;

(e) first wiring that is formed on the outside of, and adjacent to, said plurality of word lines connected to said first MISFET's, said first wiring extending in the same direction as said word lines, and being composed of the same material as said word lines; and

(f) second wiring formed adjacent to the word lines that are connected to said second MISFET's, said second wiring extending in the same direction as said word lines, and being composed of the same material as said word lines.

The present invention willnow be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a plan view showing a chip layout of a dynamic RAM to which the present invention is adapted;

Figure 2 is a plan view showing a portion of a memory cell array of the dynamic RAM of Figure 1;

Figures 3 and 4 are a sectional view taken along the line III-III of Figure 2, for illustrating the structure of a memory cell in the dynamic RAM; and a circuit diagram, respectively;

Figure 5 is a sectional view along the

line V-V of Figure 2, illustrating the formation of resist film at an end of the memory cell array;

Figure 6 is a plan view showing a portion of a dummy cell array in the dynamic RAM of Figure 1; and

Figures 7 and 8 are a circuit diagram of a dummy cell in the dynamic RAM, and a sectional view along the line VIII-VIII of Figure 6, showing the structure of the dummy cell.

Referring first to Figure 1, the dynamic RAM includes, four memory cell arrays which are formed on a silicon chip 1 which is a semiconductor chip, the memory cell arrays 2A, 2B, 2C and 2D being separated from each other in the chip 1. Among the memory cell arrays 2A to 2D are arranged X-decoders 3A, 3B and Y-decoders 4A, 4B, and at a crossing point thereof is arranged a column/row switching circuit 5. The memory cell arrays 2A to 2D contain redundancy circuits 10A, 10B, 10C and 10D that correspond to four word lines on the side portions of the Y-decoders. Dummy cell arrays 6A, 6B, 6C and 6D, as well as sense amplifiers 7A, 7B, 7C and 7D are arranged between the memory arrays and the Y-decoders. Further, around the periphery of the chip 1 are arranged bonding pads 9 and peripheral circuits 8 that include input/output buffers, and signal generator circuits.

The aforementioned additional word lines 11 for preventing the thickness of the photoresist film from decreasing are arranged at the ends of memory cell arrays close to the scribe lines, at the ends of memory cell arrays on the side of redundancy circuits 10, and in the dummy cell arrays 6.

The additional word lines in the memory cell arrays will first be described below in conjunction with Fig. 2 which illustrates on an enlarged scale a portion of the memory cell array 2A. For easy comprehension of the drawing, the insulating film among the conductor layers and the final protective film are not shown.

As will be understood from Fig. 2, a number of memory cells in the form of a matrix are arranged in the memory cell array 2A. The same also holds true for other memory cell arrays 2B, 2C and 2D. Therefore, word lines WL_0 to WL_4 extend in parallel with each other on the memory cell array. On the word lines, data lines DL_0 to DL_3, ... extend parallel to each other and at right angles to the word lines. For easy comprehension of the drawing, the data lines are shown only partially.

Memory cells are arranged at intersecting points of the word lines WL_0 to WL_4, and data lines DL_0 to DL_3.

The memory cell of dynamic RAM comprises, as shown in Figure 4, of a MISFET Q and a capacitor C for storing data that is connected to the MISFET Q.

As shown in Figure 3, the MISFET Q comprises n^+-type semiconductor regions 22 that serve as source region and drain regions, a thin silicon dioxide film 19 that serves as a gate insulating film, and a gate electrode which is a portion of a word line WL made up of polycrystalline silicon 20 and molybdenum silicide 21, that are all formed in the surface of a semiconductor substrate 12 (semiconductor chip 1) composed of a p-type single crystalline silicon.

A capacitor C comprises an n-type semiconductor region 15 that serves as an electrode, a thin insulating film 16 that serves as a di-electric layer, and a first polycrystalline silicon layer 17 which is formed on the insulating film 16 and which serves as another electrode, that are all formed in the surface of the semiconductor substrate 12. The data lines (not shown) on the intermediate insulating film 24 are electrically connected to

the n^+-type semiconductor region 22 via contact holes 25.

A field insulating film 13 is formed by selectively and thermally oxidizing the semiconductor substrate 12. A p^+-type channel stopper 14 is formed under the field insulating film 13. An intermediate insulating film 18 is formed by oxidizing the surface of the polycrystalline silicon layer 17.

In Figure 2, aluminium wiring 28 supplies a power-source voltage V_{CC} (5 volts) to the polycrystalline silicon layer 17 which serves as one electrode of the capacitor C. Wiring 28 is formed simultaneously with the data lines and extends in the same direction as the data lines. Wiring 28 is electrically connected to the polycrystalline silicon layer 17 through contact holes 27.

When another fixed potential such as earth potential (0 volts) is to be supplied to the polycrystalline silicon layer 17, a potential of 0 volts is applied to wiring 28.

The left side of the memory cell array 2A adjoins a guard ring region 29 which comprises an n^+-type semiconductor region and which is formed so as to surround the outer periphery of the memory cell arrays 2A, 2B, 2C and 2D, so that the memory cells will not be affected by the minority carriers.

The word lines WL_0 to WL_4, ... extend downward in Fig. 2, and are connected to the X-decoder 3A. Each word line is served with a low level or high level signal via the X-decoder to select a memory cell.

The data lines DL_0 to DL_3, ... extend to the right in Fig. 2, and are connected to the dummy cell array 6A, sense amplifier 7A, and Y-decoder 4A.

An additional word line WL_{ADD1} (11) is formed at an end of the memory cell array 2A, i.e., on the outside of the word line WL_0 of the extreme end. The additional word line WL_{ADD1} is formed simultaneously with the formation of word lines WL_0 to WL_4, ... The additional word line WL_{ADD1} prevents the word line WL_0 from being broken or deformed at the time of forming the contact holes 25. In other words, the additional word line

prevents the resist film for forming contact holes 25 from becoming thin on the word line WL_0.

Fig. 5 shows the shape of the resist film 26 for forming contact holes. Fig. 5 is a section view along the line V-V of Fig. 2 to which the resist film 26 is just fitted. Since the additional word line WL_{ADD1} prevents the resist film 26 from flowing to the left in Fig. 5, the resist film 26 is allowed to have a thickness on the word line WL_0 that is the same as that of the resist film 26 on other word lines. When the contact holes 25 are to be formed, therefore, the resist film 26 works sufficiently as a mask for dry etching even on the word line WL_0.

When the additional word line WL_{ADD1} is not formed, the resist film 26 assumes the shape as indicated by the dotted line in Fig. 5. The resist film 26 has a thickness on the word line WL_0 which is about one-third the thickness of the resist film on other word lines.

As mentioned earlier, thickness of the resist film varies depending upon the underlying pattern. Formation of the additional word line WL_{ADD1} makes the pattern condition around the word line WL_0 at the extreme end nearly the same as the pattern

condition around other word lines. This helps prevent the word line WL_0 from breaking or from being deformed.

Another additional word line WL_{ADD2} has also been formed at an end of the memory cell array 2A on the side of the Y-decoder. Like the above-mentioned additional word lines WL_{ADD1}, the additional word line WL_{ADD2} helps prevent the neighboring word line WL_{R3} in the memory cell array 2A from breaking or from being deformed.

The word line WL_{R3} is a part of the redundancy circuit 10A which is formed contiguous to the memory cells in the memory cell array 2A. The redundancy circuit 10A has four spare rows (redundancy rows), each spare row being provided with a word line and a memory cell connected to the word line. Among four word lines of the redundancy circuit 10A, the word line WL_{R3} is located on the side closest to the Y-decoder. This condition is nearly the same as that of the word line WL_0.

By preventing the word line WL_{R3} from breaking or from being deformed, the redundancy circuit 10A can be effectively utilized, and reliability of the semiconductor memory device can be increased. The redundancy circuit which is to substitute for

defective memory cells has fewer defects, and the substitution can be effected reliably and efficiently.

A fixed potential is applied to the additional word lines WL_{ADD1} and WL_{ADD2}. The additional word lines are quite irrelevant to such operations as writing or reading the memory cells or storing the data. It is, however, desired to prevent the additional word lines from floating as far as this is possible. As shown in Fig. 2, therefore, the additional word lines WL_{ADD1} and WL_{ADD2} have been connected to earth potential (0 volts).

Another fixed potential, such as the potential which is applied to the polycrystalline silicon layer 17, may be applied to the additional word lines.

Owing to the provision of additional word lines, there is formed as shown in Fig. 2 a MISFET Q_{ADD} to which one terminal is connected a capacitor C_{ADD} having the structure same as that of the capacitor C of a memory cell. No matter what potential the additional word lines WL_{ADD} may assume, one terminal of the capacitor C_{ADD} must be electrically connected to the guard ring 29. The minority carriers must be discharged into the

guard ring 29, so that minority carriers trapped in the n-type region 15 of the capacitor C_{ADD} will not adversely affect the capacitor of the neighboring memory cell.

Therefore, an n-type region is formed in the channel region of MISFET Q_{ADD} simultaneously with the formation of the n-type region 15. Arsenic ions that serve as n-type impurities should be implanted through the silicon oxide film 16. In the step of ion implantation, a silicon oxide film 16 is formed on the channel region of the MISFET Q_{ADD}.

In Fig. 2, furthermore, n-type regions must also be formed in the portions where the word lines WL_0, to WL_4, ..., WL_R, WL_{ADD}, ... traverse the guard ring 29.

Additional word lines WL_{ADD} (11) are also formed in other memory cell arrays 2B, 2C and 2D, as shown in Fig. 2.

Additional word lines WL_{ADD3} and WL_{ADD4} are formed in a dummy cell array 6A as shown in Fig. 6 which is a diagram to illustrate on an enlarged scale a portion of the dummy cell array 6A. For easy comprehension of the drawing, the insulating film among the conductors and the final protective

film are not shown.

In Fig. 6, dummy cells are arranged in two rows in the dummy cell array 6A. Data lines DL_0 to DL_3, ... shown in Fig. 2 extend on the dummy cell array 6A, and a dummy cell is provided for each of the data lines. A word line DWL for selecting a dummy cell and a wiring 30 that serves as a gate electrode of MISFET Q_{DC} are formed in a direction to meet the data lines at right angles therewith.

As shown in Fig. 7, the dummy cell comprises a MISFET Q_D, a capacitor C_D, and a MISFET Q_{DC} for discharging the electric charge stored in the capacitor C_D.

The MISFET's Q_D and Q_{DC} are formed through the steps for forming the MISFET's Q of memory cells, and the capacitor C_D is formed through the steps for forming the capacitors C of memory cells. Therefore, there is obtained a dummy cell of the structure which is shown in Fig. 8.

An n^+-type semiconductor region 33 is used as wiring to supply earth potential (0 volts) to the MISFET Q_{DC}. Wiring 31 contacts semiconductor region 33 via a contact hole 32 and works to reduce the resistance thereof. Semiconductor

region 33 is supplied with earth potential via aluminium wiring 34.

Wiring 28 is connected via contact hole 27 to the polycrystalline silicon layer 17 which serves as one electrode of capacitor C_D.

The additional word line WL_{ADD3} is formed between the word line DWL and wiring 30 extending nearly in parallel therewith. The additional word line WL_{ADD3} works chiefly to prevent the word line DWL_1 from breaking or from becoming deformed. The additional word line WL_{ADD4} is also provided for the same reason. By forming the additional word lines WL_{ADD3} and WL_{ADD4}, the thickness of the resist film on the word lines DWL_1 and DWL_2 can be maintained for forming contact holes 25.

Earth potential (0 volts) is applied to the additional word lines WL_{ADD3} and WL_{ADD4} via aluminium wiring 34. As mentioned earlier, other fixed potentials may be applied to the additional word lines.

Additional word lines which are irrelevant to the operation of the memory circuit are arranged on the outside of the word lines that are located at the extreme ends among the word lines in a semiconductor memory

device. The additional word lines work to prevent the resist film from flowing, and the thickness of the resist film on the word lines located at the extreme ends is prevented from being reduced. This makes it possible to effectively solve the problem of breakage in the word line that stems from the decrease in the thickness of resist film.

Additional word lines can be formed through the steps of forming the other word lines; hence, no additional step is required to form the additional word lines.

A number of modifications of the above described semiconductor memory device are possible.

For instance, if space permits, not only one additional word line but also a plurality of additional word lines can be provided.

The additional word lines should ideally be constructed in the same manner as the other word lines, and should also be made of the same material as the other word lines. Therefore, the additional word lines may be formed by using, for example, a polycrystalline silicon film, a high-melting point metal film (such as molybdenum, titanium, tantalum, tungsten), or a silicide film of high-melting point metal.

The present invention can further be adapted to a semiconductor memory device which has two or eight memory cell arrays.

Although the foregoing description has chiefly dealt with the case where the invention has been applied to a dynamic RAM, it should be noted that the invention is in no lay limited thereto.

The invention can be applied not only to a dynamic RAM but also to any other semiconductor memory device. The invention can be extensively applied to semiconductor memory devices having memory cell arrays that consist of a plurality of memory cells.

The present invention is effective for semiconductor devices in which word lines are formed by a second conductor layer that is formed on a semiconductor substrate. The invention is particularly effective for EPROM's in which the word lines are formed on the floating gates. The additional word lines should preferably have the same shape as that of other word lines. Therefore, the floating gate should also be formed under the additional word lines.

CLAIMS.

1. A semiconductor memory device including:

(a) memory cell arrays including a plurality of memory cells that are formed in rows and in columns on a semiconductor substrate;

(b) a plurality of data lines comprised of an aluminium layer, said data lines being formed in columns and coupled to said memory cells that are arrayed in corresponding columns;

(c) a plurality of word lines comprised of polycrystalline silicon and a molybdenum silicide, said word lines being formed in rows and coupled to said memory cells that are arrayed in corresponding rows; and

(d) wiring which is formed on the outside of, and adjacent to, said plurality of word lines formed in rows, said wiring extending in the same direction as said word lines, being composed of the same material as said word lines, and being formed simultaneously with the formation of the word lines.

2. A semiconductor memory device according to claim 1, wherein said wiring is supplied with a fixed potential.

3. A semiconductor memory device according to claim 1, wherein the distance between said wiring and the neighboring word line is the same as the distance between said word lines.

4. A semiconductor memory device according to claim 1, wherein each of said memory cells includes a capacitor for storing an electric charge, and a MISFET connected in series therewith, the arrangement being such that the plurality of data lines formed in columns are coupled to said MISFET's which are arrayed in corresponding columns, and the plurality of word lines formed in rows are coupled to said MISFET's that are arrayed in corresponding rows.

5. A semiconductor memory device according to claim 4, wherein said wiring is supplied with a fixed potential.

6. A semiconductor memory device according to claim 4, wherein the distance between said wiring and the neighboring word line is the same as the distance between said word lines.

7. A semiconductor memory device according to claim 5, wherein said capacitor has, as its one electrode, a conductor layer formed over said semiconductor substrate, said conductor layer serves as a common electrode for the memory cells in said memory cell array, portions of said word lines and portions of said wiring are formed over said conductor layer, other portions of said wiring extend on a thin insulating film formed on said semiconductor substrate, and first

semiconductor regions of the same conductivity type as the source and drain regions of said MISFET are formed on the surface of said semiconductor substrate in portions adjoining said wiring on said thin insulating film.

8. A semiconductor memory device according to claim 7, wherein at least one of said first semiconductor regions is connected to a guard ring that is provided adjoining to said memory cell arrays.

9. A semiconductor memory device including:

(a) memory cell arrays including a plurality of memory cells that are formed in rows and in columns on a semiconductor substrate, each of said memory cells including a first capacitor for storing an electric charge, and a first MISFET connected in series therewith;

(b) dummy cell arrays including a plurality of dummy cells that are formed on the semiconductor substrate and that generate a reference level, each of said dummy cells including a second capacitor for storing an electric charge, a second MISFET connected in series therewith, and a third MISFET for discharging the electric charge stored therein into said second capacitor;

(c) a plurality of data lines formed in columns said data lines being coupled to said first

MISFET's and said second MISFET's that are arrayed in corresponding columns;

(d) a plurality of word lines formed in rows, said word lines being coupled to said first MISFET's and said second MISFET's that are arrayed in corresponding rows;

(e) first wiring that is formed on the outside of, and adjacent to, said plurality of word lines connected to said first MISFET's, said first wiring extending in the same direction as said word lines, and being composed of the same material as said word lines; and

(f) second wiring formed adjacent to the word lines that are connected to said second MISFET's, said second wiring extending in the same direction as said word lines, and being composed of the same material as said word lines.

10. A semiconductor memory device according to claim 9, wherein said first and second wiring are supplied with a fixed potential.

11. A semiconductor memory device according to claim 10, wherein a distance between said first or second wiring and the neighboring word line is the same as the distance between said word lines.

12. A semiconductor memory device according to claim 10, wherein said second capacitor has, as its one electrode, a conductor layer that is formed

on said semiconductor substrate, said conductor layer serving as a common electrode for a plurality of dummy cells, portions of said word lines connected to said second MISFET's being formed on said conductor layer, and said second wiring being formed on said conductor layer.

13. A semiconductor memory device according to claim 12, wherein third wiring connected to said third MISFET's is formed adjacent to the word lines connected to said second MISFET's in a region where said conductor layer does not exist, said third wiring extending in the same direction as said word lines and being composed of the same material as said word lines, and said second wiring being provided between the word lines connected to said second MISFET's and said third wiring.

14. A semiconductor memory device constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.
