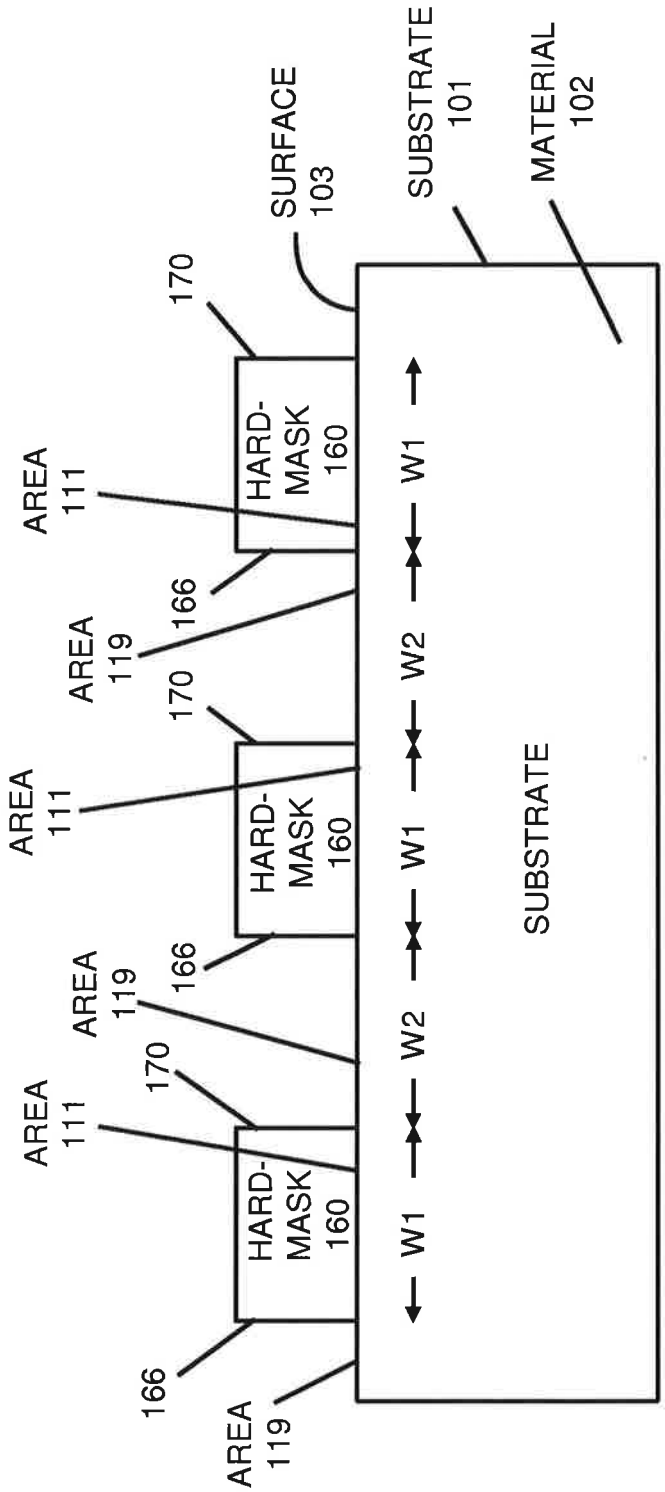

SURFACE 103
SUBSTRATE 101
MATERIAL 102
170
HARD-MASK 160
AREA 111
166
AREA 119
W1
W2
SUBSTRATE

FIG. 1

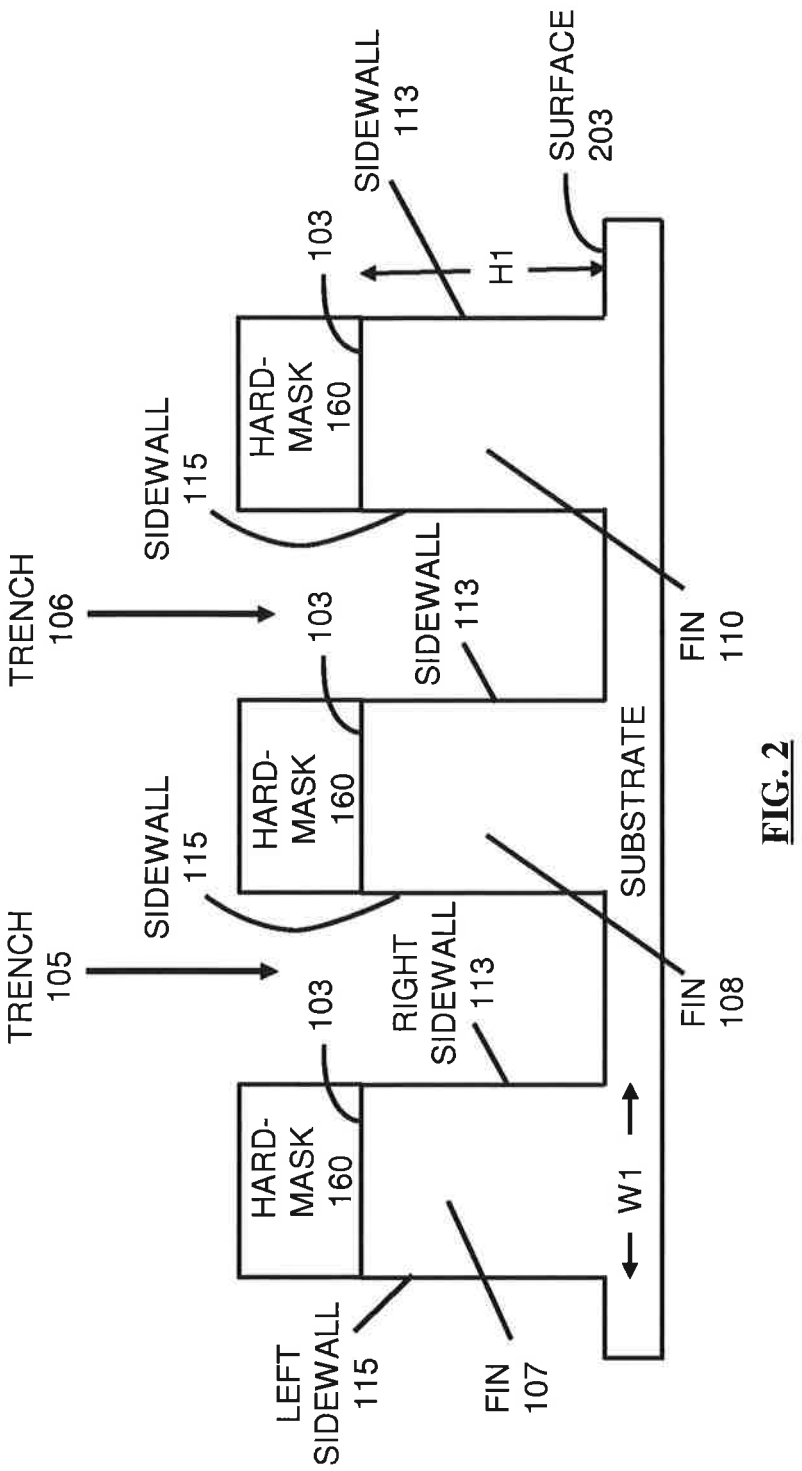

SURFACE 203
SIDEWALL 113
H1
103
HARD-MASK 160
SIDEWALL 115
TRENCH 106
SIDEWALL 113
FIN 110
SUBSTRATE
SIDEWALL 115
TRENCH 105
RIGHT SIDEWALL 113
FIN 108
W1
LEFT SIDEWALL 115
FIN 107

FIG. 2

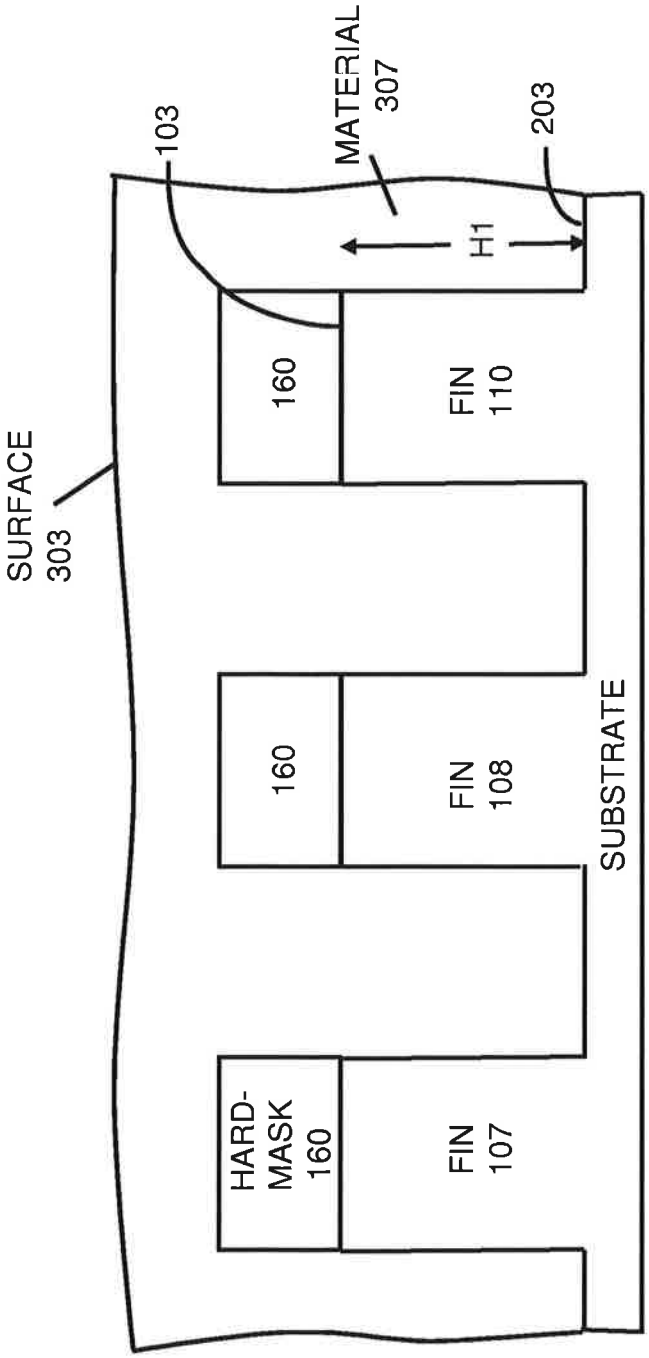

SURFACE
303
103
MATERIAL
307
203
H1
160
FIN
110
160
FIN
108
HARD-
MASK
160
FIN
107
SUBSTRATE

FIG. 3

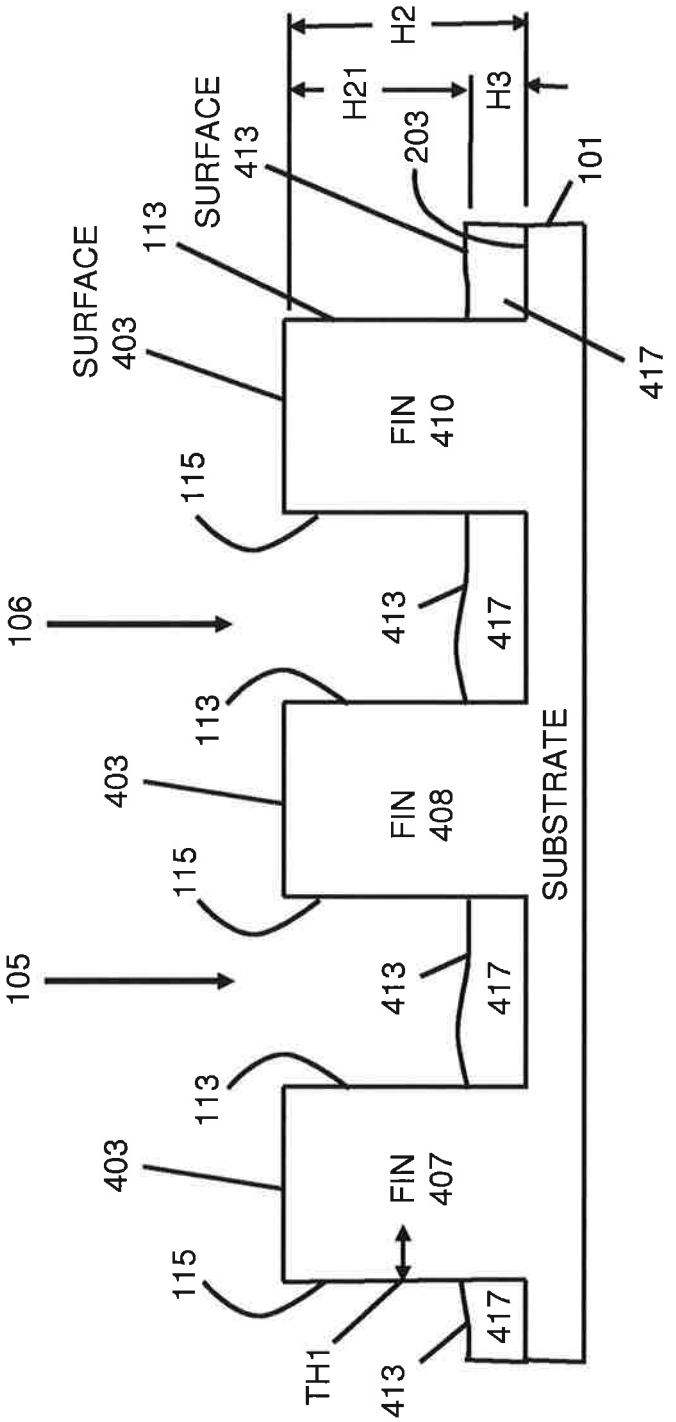

H2
H21
H3
203
101
SURFACE
413
SURFACE
403
113
417
FIN
410
115
106
413
417
113
403
FIN
408
115
105
SUBSTRATE
413
417
113
403
FIN
407
115
TH1
413
417

FIG. 4

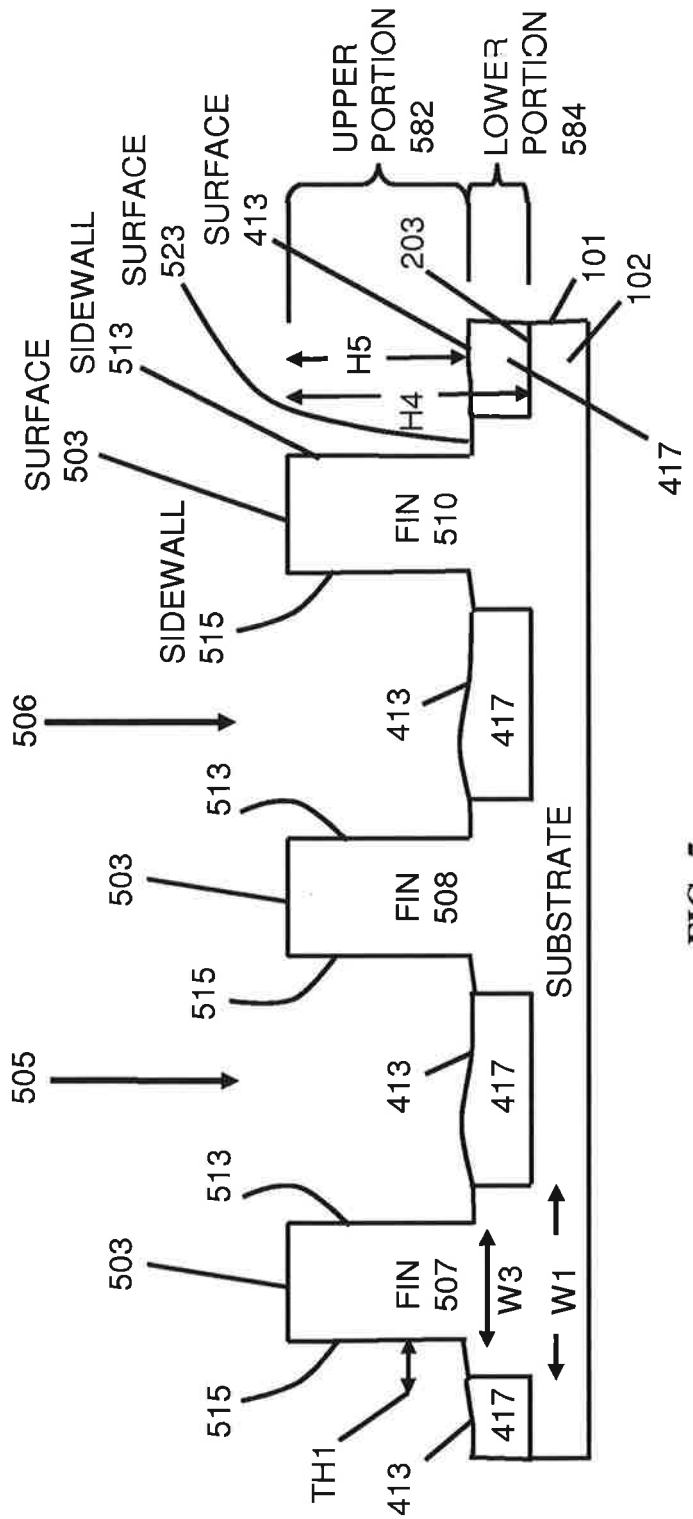

UPPER PORTION 582
LOWER PORTION 584
SURFACE 413
SURFACE 523
SIDEWALL 513
SURFACE 503
SIDEWALL 515
203
101
102
H5
H4
417
FIN 510
FIN 508
FIN 507
506
505
413
417
503
513
515
SUBSTRATE
W3
W1
TH1

FIG. 5

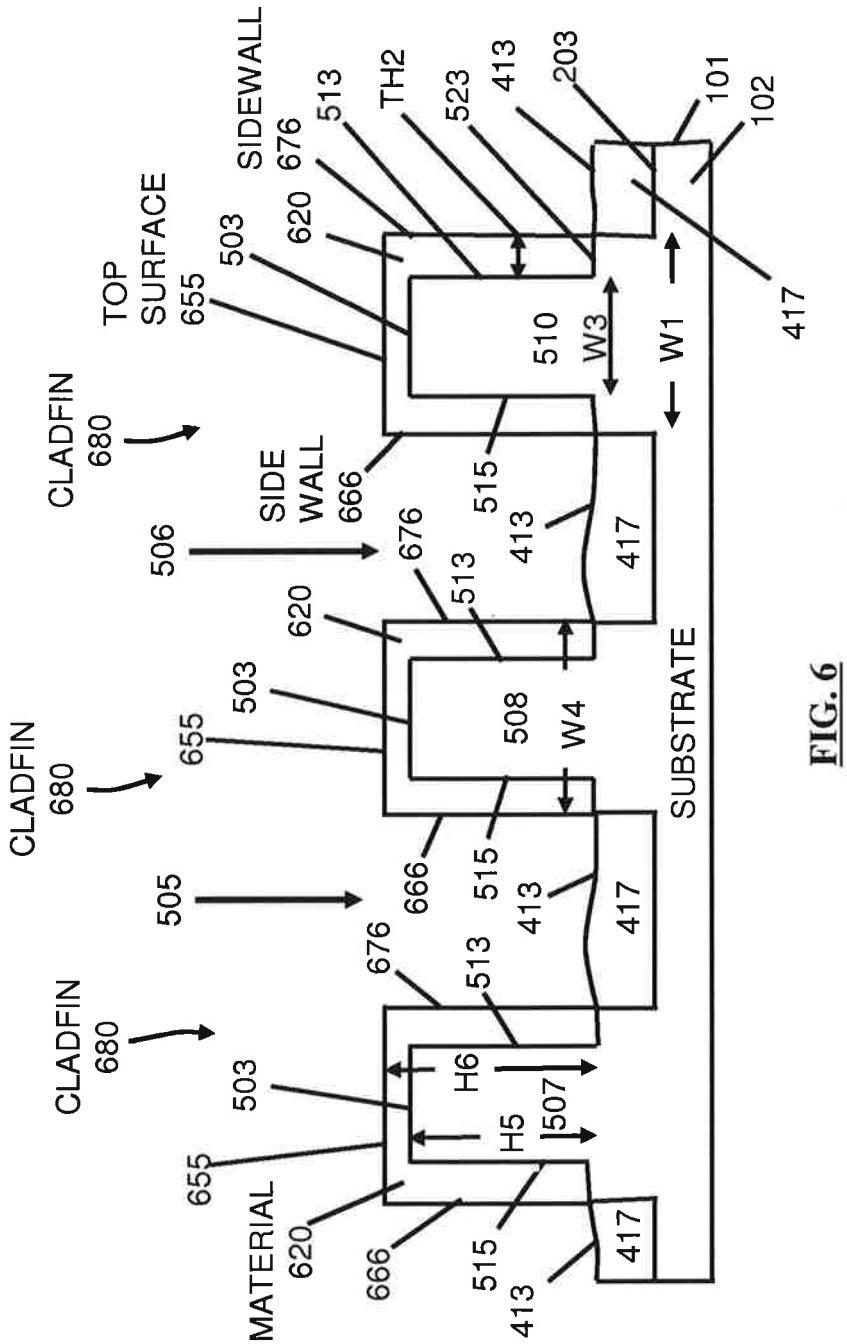

CLADFIN
680
CLADFIN
680
CLADFIN
680
TOP SURFACE
SIDE WALL
SIDEWALL
SUBSTRATE
MATERIAL
503
655
620
676
513
TH2
523
413
203
101
102
417
510
W3
W1
506
505
666
515
508
W4
H6
H5
507

FIG. 6

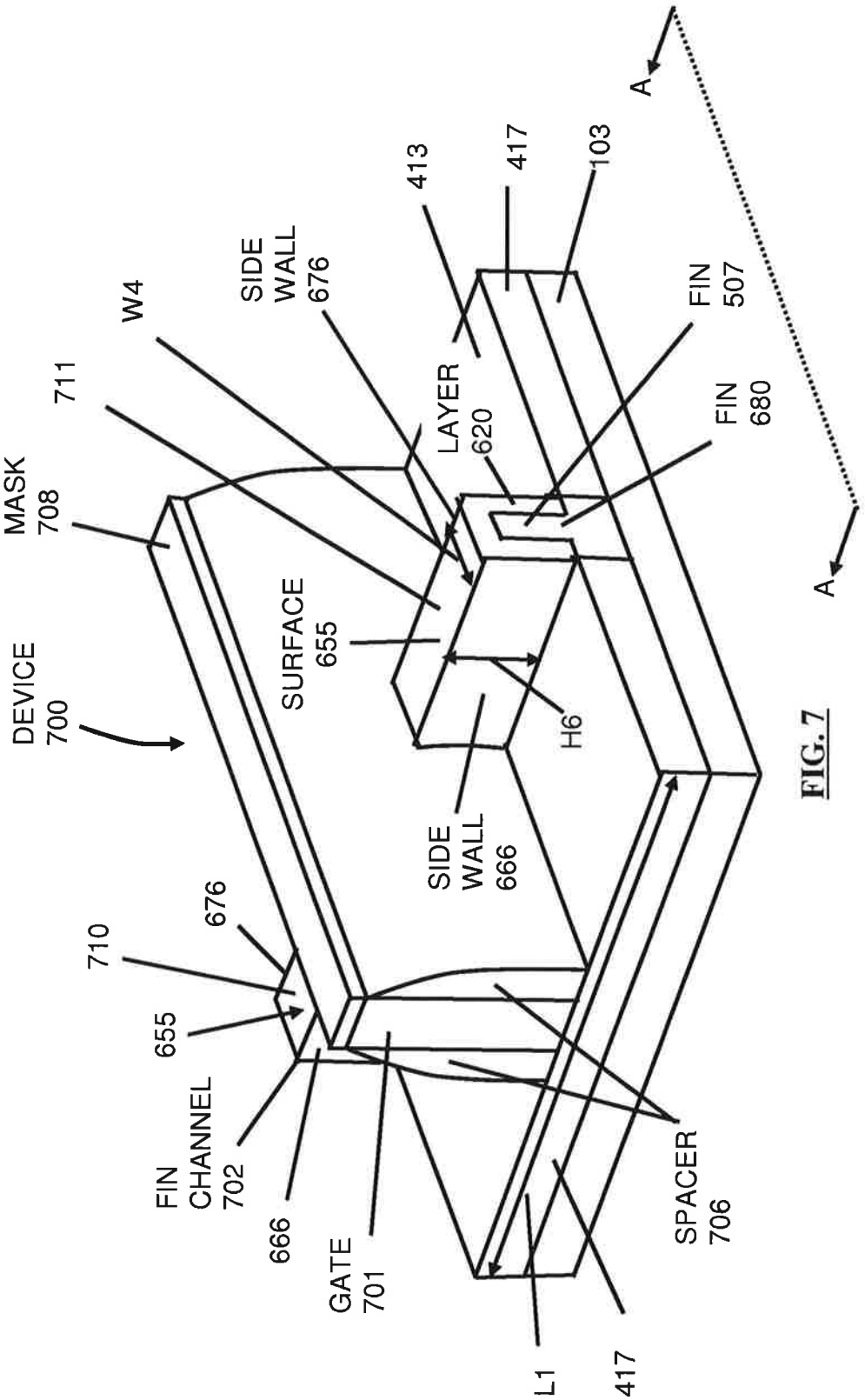

A
A
413
417
103
SIDE WALL 676
W4
711
MASK 708
DEVICE 700
SURFACE 655
LAYER 620
FIN 507
FIN 680
H6
SIDE WALL 666
676
710
655
FIN CHANNEL 702
666
GATE 701
L1
417
SPACER 706

FIG. 7

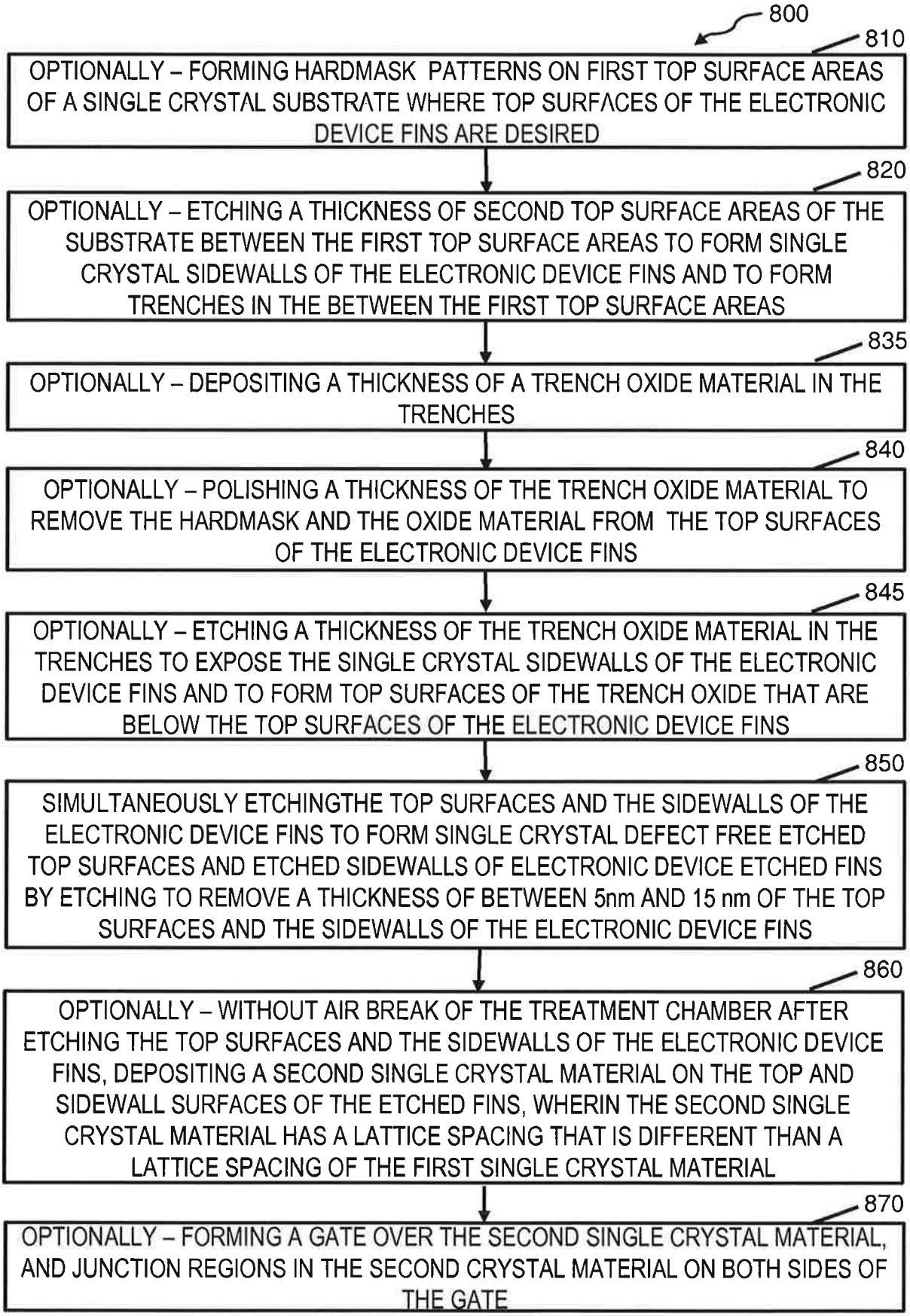

800
810
OPTIONALLY – FORMING HARDMASK PATTERNS ON FIRST TOP SURFACE AREAS OF A SINGLE CRYSTAL SUBSTRATE WHERE TOP SURFACES OF THE ELECTRONIC DEVICE FINS ARE DESIRED
820
OPTIONALLY – ETCHING A THICKNESS OF SECOND TOP SURFACE AREAS OF THE SUBSTRATE BETWEEN THE FIRST TOP SURFACE AREAS TO FORM SINGLE CRYSTAL SIDEWALLS OF THE ELECTRONIC DEVICE FINS AND TO FORM TRENCHES IN THE BETWEEN THE FIRST TOP SURFACE AREAS
835
OPTIONALLY – DEPOSITING A THICKNESS OF A TRENCH OXIDE MATERIAL IN THE TRENCHES
840
OPTIONALLY – POLISHING A THICKNESS OF THE TRENCH OXIDE MATERIAL TO REMOVE THE HARDMASK AND THE OXIDE MATERIAL FROM THE TOP SURFACES OF THE ELECTRONIC DEVICE FINS
845
OPTIONALLY – ETCHING A THICKNESS OF THE TRENCH OXIDE MATERIAL IN THE TRENCHES TO EXPOSE THE SINGLE CRYSTAL SIDEWALLS OF THE ELECTRONIC DEVICE FINS AND TO FORM TOP SURFACES OF THE TRENCH OXIDE THAT ARE BELOW THE TOP SURFACES OF THE ELECTRONIC DEVICE FINS
850
SIMULTANEOUSLY ETCHINGTHE TOP SURFACES AND THE SIDEWALLS OF THE ELECTRONIC DEVICE FINS TO FORM SINGLE CRYSTAL DEFECT FREE ETCHED TOP SURFACES AND ETCHED SIDEWALLS OF ELECTRONIC DEVICE ETCHED FINS BY ETCHING TO REMOVE A THICKNESS OF BETWEEN 5nm AND 15 nm OF THE TOP SURFACES AND THE SIDEWALLS OF THE ELECTRONIC DEVICE FINS
860
OPTIONALLY – WITHOUT AIR BREAK OF THE TREATMENT CHAMBER AFTER ETCHING THE TOP SURFACES AND THE SIDEWALLS OF THE ELECTRONIC DEVICE FINS, DEPOSITING A SECOND SINGLE CRYSTAL MATERIAL ON THE TOP AND SIDEWALL SURFACES OF THE ETCHED FINS, WHERIN THE SECOND SINGLE CRYSTAL MATERIAL HAS A LATTICE SPACING THAT IS DIFFERENT THAN A LATTICE SPACING OF THE FIRST SINGLE CRYSTAL MATERIAL
870
OPTIONALLY – FORMING A GATE OVER THE SECOND SINGLE CRYSTAL MATERIAL, AND JUNCTION REGIONS IN THE SECOND CRYSTAL MATERIAL ON BOTH SIDES OF THE GATE

FIG. 8

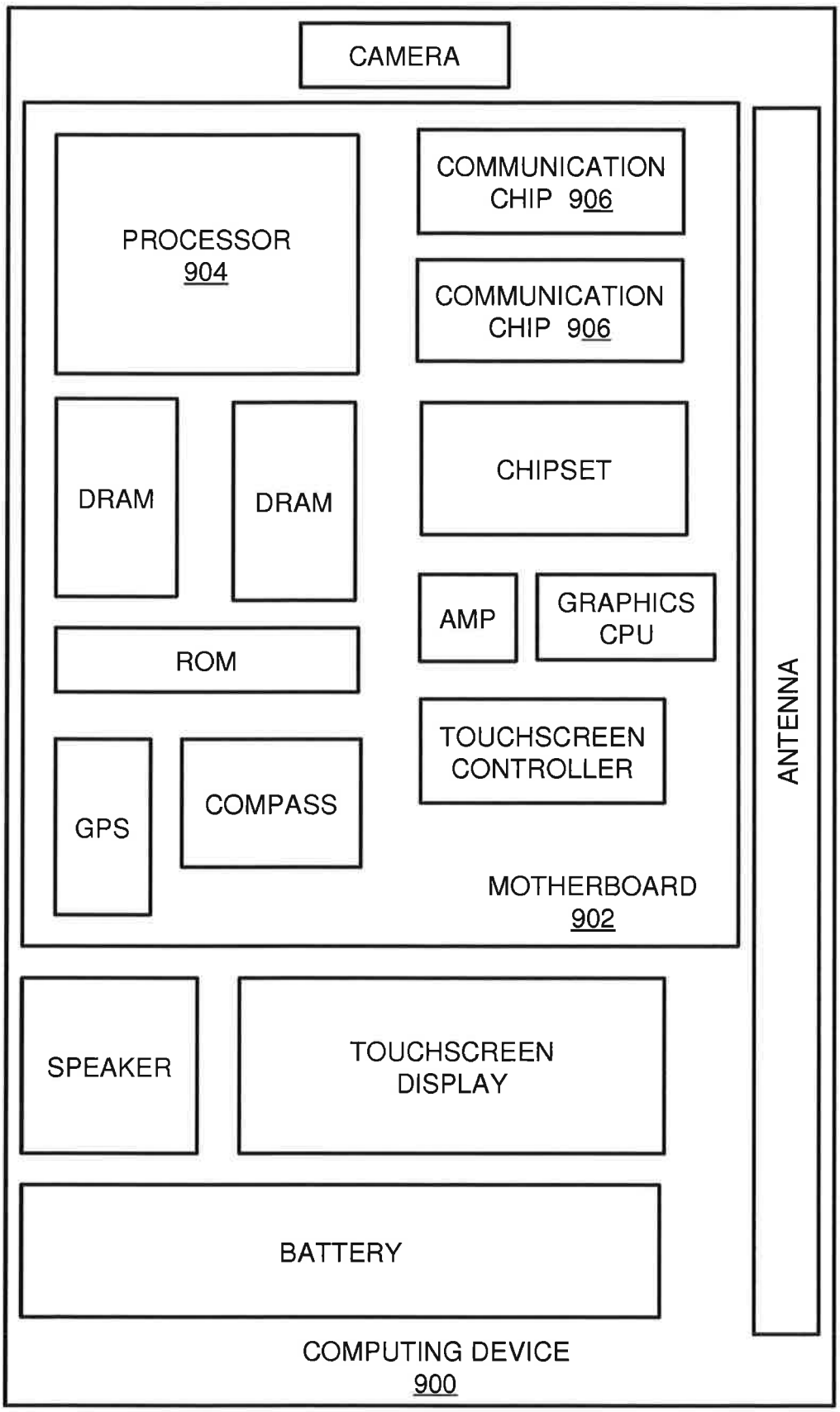

CAMERA
PROCESSOR
904
COMMUNICATION
CHIP 906
COMMUNICATION
CHIP 906
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
902
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
900

FIG. 9