

The invention relates to a phase control circuit.

Prior Art

Present-day television receivers use a PLL control device (phase locked loop) for the line synchronization in the horizontal oscillator. The horizontal oscillator produces a Phil-signal with the frequency of the horizontal synchronization pulse (H-Sync) but with a different mark-space ratio.

If, for example, a different programme source is switched on or a programme change occurs, the line synchronization in the horizontal oscillator is to take place as rapidly as possible in order for example to avoid a distorted picture which is disturbing to the observer and in order rapidly to bring assemblies in the television receiver which are controlled by the Phil-signal into a determinate operating state.

In order to ensure a good control response of the PLL in the locked state, the characteristic curve of the PLL control device is to possess specific properties, for example a relatively greater control time constant in order for example that noise superimposed upon a television signal does not produce a jitter in the PLL control circuit in spite of the fundamental precise timing of the synchronization pulses.

In the unlocked state, however, the control operation of the PLL is to be rapid, for which purpose a small control time constant is in fact required. However, because the H-Sync (e.g. $4.7 \mu\text{s}$) is relatively short compared to the line duration (e.g. $64 \mu\text{s}$), the control response of the PLL is non-linear (mark-space ratio of the PLL input signals 4.7 : 64). Consequently in a large phase range the control speed

is independent of the amount of the phase difference and the control operation of the PLL is relatively slow in the case of relatively larger phase differences even when a time constant switch-over is effected in the VCR mode (3-times faster).

Fig. 1 illustrates a known PLL control circuit. A phase comparator 11 is shown which is supplied with the H-Sync and the Phil-signal as input signals. The output of the phase comparator 11 comprises a current source for the control current 14. This control current is low-pass-filtered in the loop filter 12 and fed to a VCO (voltage controlled oscillator) 13. The VCO 13 comprises a frequency divider and at its output supplies the Phil-signal with line frequency (e.g. 15.625 KHz). In the locked state H-Sync and Phil-signal are coupled in phase-locked fashion.

Fig. 2 shows the H-Sync, the Phil-signal and the control current 14 (I_{out}). The left-hand half of the Figure shows the locked state. The Phil-signal and the H-Sync have a phase difference $\Delta\phi$ of $+90^\circ$ and -90° and the resultant average control current has the value 0. The right-hand half of the Figure shows an unlocked state. In large phase difference ranges the amount of the control current 14 is independent of the phase position of the Phil-signal.

This relationship is illustrated in Fig. 3 (solid line). Only in relatively small phase difference ranges of $\Delta\phi$ (approximately $-103^\circ \dots -77^\circ$, $77^\circ \dots 103^\circ$) does this average control current $\overline{I_{out}}$ change in dependence upon the phase difference of the Phil-signal, i.e. a greater phase difference gives rise to a larger average control current $\overline{I_{out}}$.

In the range from $-77^\circ \dots 77^\circ$ a large phase difference of the Phil-signal leads only to a relatively small constant

average control current $\overline{I_{out}}$, although with a larger phase difference it ought to become greater. Thus it takes a relatively long time until a relatively large phase difference is controlled by the PLL. This leads to the above mentioned disadvantages. On the other hand, a general increase in the control current I_4 leads to an unfavourable control response in the locked state in the case of a noisy input signal. Furthermore, too great a general increase in the average control current can lead to the oscillation of the control circuit.

EP-A-0 314 219 has described a PLL for two logic signals of the same frequency wherein at least one of the two signals has a mark-space ratio differing from 50:50. In the event of relatively larger phase differences the amplitude of the control signal is increased by the switching over of the loop amplification.

In US-A-4 214 260 a pulse widening is carried out which, however, serves only as a masking means for the purpose of noise suppression in the event of non-synchronization.

Invention

The aim of the invention is, even in the case of a relatively large phase difference between the H-Sync and the Phil-signal to facilitate a rapid control operation of the PLL without changing the control characteristic of the PLL in the locked state.

This aim is fulfilled by the features described in Claim 1. Advantageous further developments of the invention are described in the sub-claims.

An ideal characteristic curve would be that shown in broken lines in Fig. 3, as is always provided in conventional PLL

circuits (mark-space ratio of the input signals 1:1). The control current for the VCO is increased by a specific factor in an extended phase difference range (in the non-linear part of the PLL control characteristic). For this purpose a line-synchronous LRI (line retrace inhibit) pulse is utilized which is present in many present-day television receivers and which has an extended pulse duration compared to the H-Sync and for example suppresses interference signals during the non-visible part of the lines. Instead of the LRI pulse it is also possible to use any other line-synchronous pulse which has an extended pulse duration compared to the H-Sync.

Drawings

In the following an exemplary embodiment of the invention will be explained making reference to drawings in which:

- Fig. 1 illustrates a PLL circuit in a horizontal oscillator (known),
- Fig. 2 is a time diagram of input and output signals of the phase comparator in the PLL (known),
- Fig. 3 shows the characteristic curve for the average output current of the phase comparator as a function of the phase difference of the input signals (known),
- Fig. 4 is a diagram of a PLL circuit according to the invention in a horizontal oscillator,
- Fig. 5 is a time diagram of input- and output signals of the phase comparator in the PLL circuit according to the invention,
- Fig. 6 is the characteristic curve according to the invention for the average output current of the phase comparator as a function of the phase difference of the input signals.

Figs. 1 to 3 have already been described in the foregoing.

Exemplary Embodiments

Fig. 4 illustrates a phase comparator 41 which receives, as input signal, the H-Sync, the Phil-signal and a LRI signal. The output of the phase comparator 41 contains a controllable current source for the control current 44. This control current is low-pass-filtered in the loop filter 42 and conveyed to a VCO 43. The VCO 43 supplies for example a 500 KHz-signal at its output. In a following logic- and frequency divider circuit 47 for example the LRI signal is generated and the Phil-signal with line frequency (e.g. 15.625 KHz). As mentioned above, the LRI signal is already present in many televisions. On the other hand it is easy for those skilled in the art to derive the LRI signal from other signals in the television. This can take place by calling up counter readings in the frequency divider circuit.

If no H-Sync is present, for example in the case of the reproduction of videotext pages stored in the television device at the end of transmission, the switch 45 switches over to a specified control voltage 46. The information required for this purpose (no H-Sync present) is generated in the H-Sync recognition circuit 49.

In the case of the reproduction of a video-recorder signal, for example the control current in the controllable current source in the phase comparator 41 can be increased by the factor three to facilitate a better control of fluctuations in synchronism of the video-recorder or frames reproduced with different lengths (approx. $\pm 1 \mu s$). The information relating to the video-recorder operation can be supplied to the phase comparator 41 for example from a SCART socket.

In a lock detector 40, which is supplied with the H-Sync and the Phil-signal as input signals, it is now determined whether the PLL has locked. In the locked state H-Sync and Phil-signal are coupled in phase-locked fashion and the switch 48 is open. In the unlocked state the switch 48 is closed and the control current is increased by a factor, for example, of four in the control source. As a result the PLL can more rapidly control a phase deviation of the Phil-signal from the H-Sync.

Fig. 5 illustrates the H-Sync 53, 55, the Phil-signal 51, the LRI-signal 52 and the control current 54, 56 (I_{out}). The upper part of the Figure shows the locked state. The Phil-signal 51 and the H-Sync 53 possess a phase shift $\Delta\phi$ of $+90^\circ$ and -90° and the resultant average control current I_{out} has the value 0 ($+I_0$ and $-I_0$ averaged). The lower part of the Figure shows an unlocked state. During the duration of the H-Sync 55, which does not fall within the duration of the LRI pulse 52, the control current 56 (I_{out}) is increased by the factor four. If, on the other hand, the phase of the H-Sync 55 falls within the duration of the LRI-pulse 52, the control current 56 remains unchanged.

The characteristic curve, illustrated in Fig. 6, for the control current 44, 54, 56 (I_{out}) as a function of the phase difference $\Delta\phi$ results from the foregoing. In the ranges of $-103^\circ \dots -77^\circ$ and $77^\circ \dots 103^\circ$ this characteristic is identical to that shown in Fig. 3. In the ranges of approx. $<-110^\circ$, $-70^\circ \dots 70^\circ$ and $>110^\circ$ on the other hand the control current 44, 54, 56 is advantageously increased by the factor four compared to the characteristic according to Fig. 3. In operation with a video-recorder the control current can then be increased by the factor 12 ($3 \cdot 4$).

As a result of the enlarged linear range of the characteristic curve ($-110^\circ \dots -70^\circ$, $70^\circ \dots 110^\circ$) the PLL

control circuit attains almost an ideal response (broken lines), i.e. in the locked state the control response is slow and in the case of an increasing phase difference the control response becomes faster. The control response in the still remaining non-linear section ($<-110^\circ$, $-70^\circ \dots 70^\circ$, $>110^\circ$) is advantageously improved by exaggerations at -110° , -70° , 70° and 110° .

The average control current $\overline{I_{out}}$ which is formed by filtering in the loop filter 42 from the control current 44 (I_{out}), can also be changed appropriately in its amount in that the loop filter 42 is changed in respect of its transfer function, in which case the current source in the phase comparator then emits a uniform current I_{out} .

The invention can be applied not only to PLL control devices in horizontal oscillator circuits, but generally in PLL control devices with signals which do not possess the ideal mark-space ratio of 50:50.



Claims

1. A phase control circuit for at least two logic signals (H-Sync, Phil) of the same frequency, wherein at least one of the two signals (H-Sync) has a mark-space ratio differing from a mark-space ratio of 50:50, where the phase position of the signals in relation to one another can be controlled by a control signal (14, 44) and where the control signal (14, 44) changes in linear fashion in the two ranges of small phase differences ($\Delta\phi$) which extend symmetrically around the phase positions of in each case $+90^\circ$ and -90° and between these two ranges and outside of these two ranges has a component (31, 61) which remains constant in terms of amplitude and which possesses a first amplitude, characterised in that:

- with the aid of a further logic signal (LRI), the frequency of which is identical to the frequency of the two logic signals and the pulse breadth of which is distinctly greater than that of the logic signal (H-Sync) with the differing mark-space ratio, the source (α) for the control signal (44) is switched over by switching means (48), which are controlled by a lock detector (40), in such manner that between these two ranges and outside of these two ranges the control signal (44) has a component (61) which remains constant in terms of amplitude and which possesses a second amplitude increased by a specified factor;
- the source is switched over to the increased control signal when the logic signal (H-Sync) with the differing mark-space ratio and the further logic signal (LRI) are not coupled in phase-locked fashion;
- the source is switched over to the normal control signal when the phase of the logic signal (H-Sync) with the differing mark-space ratio falls within the pulse duration of the further logic signal (LRI);



- where the sections of the linear components of the control signal, which in the ranges of small phase differences ($\Delta\phi$) extend symmetrically around the phase positions of in each case $+90^\circ$ and -90° , are correspondingly enlarged.
2. A phase control circuit as claimed in Claim 1, characterised in that the ranges of small phase differences ($\Delta\phi$) between the two logic signals (H-Sync, Phil) occur at approximately $-103^\circ \dots -77^\circ$ and $77^\circ \dots 103^\circ$, and that the enlargement of these ranges comprises phase differences of approximately $-110^\circ \dots -103^\circ$, $-77^\circ \dots -70^\circ$, $70^\circ \dots 77^\circ$ and $103^\circ \dots 110^\circ$.
 3. A phase control circuit as claimed in Claim 1 or 2, characterised in that the curve for the control signal (44) exhibits a greater slope in the enlarged linear ranges than in the ranges of small phase differences.
 4. A phase control circuit as claimed in one or several of Claims 1 to 3, characterised in that the control signal (44) is a control current (44).