

Description

The invention relates to an analogue-to-digital converter circuit comprising a first analogue-to-digital converter having a comparison circuit provided with a first input for an analogue signal to be converted and a second input for an analogue reference signal originating from a first digital-to-analogue converter connected to an output of the comparison circuit and supplying a first digital signal, an amplifier also connected to the said output, and a first switch which receives a control signal after a conversion cycle of the first analogue-to-digital converter and then passes an output signal of the amplifier on to a measurement circuit comprising a second analogue-to-digital converter which supplies a second supplementary digital signal, as a result of which the accuracy of the converter circuit is increased.

Such an analogue-to-digital converter circuit is known from US—PS 3,603,970.

In order to increase the range and the resolving power of these converter circuits, it is suggested that the residual voltage which is left after a conversion cycle and which is mostly smaller than the value of the least significant bit is digitized in another analogue-to-digital converter. The digital value obtained can be used to correct any errors larger than 1 L.S.B. (least significant bit) and to increase the measuring accuracy.

It will be appreciated that these known measures can be used until a physical lower limit is reached, which in this case is determined by the value of the noise signal. This signal will have to be smaller than the value of the smallest bit in the second analogue-to-digital converter.

According to the invention, measures are suggested to digitize a residual signal of a first analogue-to-digital converter, which has a substantial noise component, the influence of the noise then being substantially completely eliminated.

For this purpose, an analogue-to-digital converter circuit of the type mentioned in the opening paragraph is characterized in that the measurement circuit includes an integrator connected to the first switch, in that the second analogue-to-digital converter is connected to an output of the integrator, in that the first switch is closed during a constant period of time between two of the said conversion cycles and in that the second analogue-to-digital converter, when a given quantization level corresponding to a value which is at most equal to the value of the least significant bit of the first analogue-to-digital converter is exceeded, connects by means of a second switch a source to the input of the integrator in order to reset the output signal of the integrator with the said level, while further provision is made of a digital adder circuit having a first input for the first digital signal, a second input for the second digital signal and an output supplying the desired digital signal.

It is then advantageous that the range of the

converter circuit can be extended into the noise. As compared with the known circuit, a few additional bits are obtained due to the noise filter method used.

In advantageous embodiments, the second analogue-to-digital converter may be threshold value detector which has a threshold value equal to the said quantization level corresponding to the least significant bit of the first analogue-to-digital converter and which, when this level is exceeded by the output signal of the integrator, gives off a -1- signal as a second digital signal, which signal keeps also the second switch closed during a constant period of time, the said source supplying current, while the first digital signal is varied by one least significant bit. It is then achieved by simple means that an accurate least significant bit is present.

The second analogue-to-digital converter may also be of the parallel type (flash encoder) having a gate circuit connected to the digital outputs of the second analogue-to-digital converter, which gate circuit determines the quantization level and produces a signal when this level is exceeded, for closing the second switch during a constant period of time, the said source supplying current.

A very rapid conversion for the second digital signal can thus be obtained, while an embodiment can further be characterized in that the said source is a second digital-to-analogue converter, whose inputs are connected to the second digital signal.

The invention will be described more fully with reference to the drawing. In the drawing:

Figure 1 shows a block circuit diagram and

Figure 2 shows a further elaboration of a circuit diagram of the converter circuit according to the invention.

In Figure 1, a first analogue-to-digital converter 1 is provided with a comparison circuit 2 having a first input 3 for an analogue signal to be converted and to be supplied to an input 4 and having a second input 5 for an analogue reference signal originating from a digital-to-analogue converter 6 which is connected to an output 7 of the comparison circuit 2 and which also supplies a first digital signal 8. An amplifier 9 is also connected to the output 7 and serves to amplify the residual signal, which is normally smaller than the value of the least significant bit of the analogue-to-digital converter 1, after termination of a conversion cycle and to pass it via a switch 10, then closed, on to a measurement circuit 11 comprising a second analogue-to-digital converter 12 which supplies a second digital signal 13. The switch 10 is closed for a constant period of time by means of a monostable circuit 14 controlled via a line 24 by a central control unit 15 which is connected by control lines 16 and 17 also to the digital-to-analogue converter 6. The measurement circuit 11 includes an integrator 18 which is connected by an input 19 to the switch 10 and is connected by an output 20 to the analogue-to-digital converter 12. The integrator 18 is composed of a resistor 21, a capacitor 22 and an amplifier 23. The

analogue-to-digital converter 12 further measures whether the signal at the output 20 exceeds a given level. This level may be equal to the value of the least significant bit of the analogue-to-digital converter 1 integrated during the constant period of time of the circuit 14. If this level is exceeded, the analogue-to-digital converter 12 supplies a signal at the line 20 which starts a monostable circuit 26, which closes for a constant period of time a second switch 27 so that a source 28 is connected to the input 19 of the integrator 18. After the time period has elapsed, the output signal at the output 20 has been reset with the said level.

For combining the two digital signals 8 and 13, a digital adder circuit 29 is provided having a first input 30 for the first digital signal 8, a second input 31 for the second digital signal 13 and an output 32 supplying the digital conversion signal of the analogue signal at the input 4. The circuit 26 is further connected through a control line 33 to the unit 15. This unit 15 may further supply other time-dependent control signals for the various units of the converter circuit.

In Figure 2, a few of the blocks shown in Figure 1 are further elaborated. The first analogue-to-digital converter 1 is of the successive approximation type. The comparison circuit 2 comprises an operational amplifier 34 having an input resistor 35 and a feedback resistor 36. The analogue-to-digital conversion part comprises a comparator 37, which is controlled from the unit 15 via a line 38 and controls a shift resistor 39, which supplies digital output information to an output 40 for a digital-to-analogue converter which is connected through a line 42 to the input 5. The digital information obtained at the output 40 after the termination of a conversion further provides the first digital signal 8.

The amplifier 9 is composed of an operational amplifier 43 having feedback resistors 44 and 45. The second analogue-to-digital converter 12 comprises a parallel encoder 46 having an output 47 for the digital information 13 and an output 48 for the same information, to which a gate circuit 49 is connected which has a coding corresponding to the quantization level.

The second analogue-to-digital converter 12 can be a threshold value detector of the kind indicated in US-PS 3,603,970 by reference numerals 18 and 21 in Figure 2. The input at resistor 17 in this Figure is then connected to the output 20 of the integrator 18 in Figure 1. of this Application and the line 191 in the known Figure is then line 13 and 25 in the said Figure 1.

The detector may also be a Schmitt trigger. The source 28 may be a digital-to-analogue converter which is connected by digital inputs to the digital outputs of the converter 46, as indicated by the broken line 51. The converter 46 is controlled through a line 50 by the unit 15.

Claims

1. An analogue-to-digital converter circuit comprising a first analogue-to-digital converter having a comparison circuit provided with a first input for an analogue signal to be converted and a second input for an analogue reference signal originating from a first digital-to-analogue converter connected to an output of the comparison circuit and supplying a first digital signal, an amplifier also connected to the said output, and a first switch which receives a control signal after a conversion cycle of the first analogue-to-digital converter and then passes an output signal of the amplifier on to a measurement circuit comprising a second analogue-to-digital converter supplying a second supplementary digital signal, as a result of which the accuracy of the converter circuit is increased, characterized in that the measurement circuit includes an integrator connected to the first switch, in that the second analogue-to-digital converter is connected to an output of the integrator, in that the first switch is closed during a constant period of time between two of the said conversion cycles and in that the second analogue-to-digital converter, when a given quantization level corresponding to a value which is at most equal to the value of the least significant bit of the first analogue-to-digital converter is exceeded, connects by means of a second switch a source to the input of the integrator in order to reset the output signal of the integrator with the said level, while further provision is made of a digital adder circuit having a first input for the first digital signal, a second input for the second digital signal and an output supplying the desired digital signal.

2. An analogue-to-digital converter circuit as claimed in Claim 1, characterized in that the second analogue-to-digital converter is a threshold value detector which has a threshold value equal to the said quantization level corresponding to the least significant bit of the first analogue-to-digital converter and which, when this level is exceeded by the output signal of the integrator, supplies a -1- signal as a second digital signal, which signal further keeps the second switch closed for a constant period of time, the said source supplying current, while the first digital signal is varied by one least significant bit.

3. An analogue-to-digital converter circuit as claimed in Claim 1, characterized in that the second analogue-to-digital converter is of the parallel type and in that a gate circuit is connected to the digital outputs of the second analogue-to-digital converter, which gate circuit determines the quantization level and supplies a signal when this level is exceeded for closing the second switch for a constant period of time, the said source supplying current.

4. An analogue-to-digital converter circuit as claimed in Claim 1 or 2, characterized in that the said source is a second digital-to-analogue converter, which is connected by its inputs to the second digital signal.

analogue-to-digital converter 12 further measures whether the signal at the output 20 exceeds a given level. This level may be equal to the value of the least significant bit of the analogue-to-digital converter 1 integrated during the constant period of time of the circuit 14. If this level is exceeded, the analogue-to-digital converter 12 supplies a signal at the line 20 which starts a monostable circuit 26, which closes for a constant period of time a second switch 27 so that a source 28 is connected to the input 19 of the integrator 18. After the time period has elapsed, the output signal at the output 20 has been reset with the said level.

For combining the two digital signals 8 and 13, a digital adder circuit 29 is provided having a first input 30 for the first digital signal 8, a second input 31 for the second digital signal 13 and an output 32 supplying the digital conversion signal of the analogue signal at the input 4. The circuit 26 is further connected through a control line 33 to the unit 15. This unit 15 may further supply other time-dependent control signals for the various units of the converter circuit.

In Figure 2, a few of the blocks shown in Figure 1 are further elaborated. The first analogue-to-digital converter 1 is of the successive approximation type. The comparison circuit 2 comprises an operational amplifier 34 having an input resistor 35 and a feedback resistor 36. The analogue-to-digital conversion part comprises a comparator 37, which is controlled from the unit 15 via a line 38 and controls a shift resistor 39, which supplies digital output information to an output 40 for a digital-to-analogue converter which is connected through a line 42 to the input 5. The digital information obtained at the output 40 after the termination of a conversion further provides the first digital signal 8.

The amplifier 9 is composed of an operational amplifier 43 having feedback resistors 44 and 45. The second analogue-to-digital converter 12 comprises a parallel encoder 46 having an output 47 for the digital information 13 and an output 48 for the same information, to which a gate circuit 49 is connected which has a coding corresponding to the quantization level.

The second analogue-to-digital converter 12 can be a threshold value detector of the kind indicated in US-PS 3,603,970 by reference numerals 18 and 21 in Figure 2. The input at resistor 17 in this Figure is then connected to the output 20 of the integrator 18 in Figure 1 of this Application and the line 191 in the known Figure is then line 13 and 25 in the said Figure 1.

The detector may also be a Schmitt trigger. The source 28 may be a digital-to-analogue converter which is connected by digital inputs to the digital outputs of the converter 46, as indicated by the broken line 51. The converter 46 is controlled through a line 50 by the unit 15.

Claims

1. An analogue-to-digital converter circuit comprising a first analogue-to-digital converter having a comparison circuit provided with a first input for an analogue signal to be converted and a second input for an analogue reference signal originating from a first digital-to-analogue converter connected to an output of the comparison circuit and supplying a first digital signal, an amplifier also connected to the said output, and a first switch which receives a control signal after a conversion cycle of the first analogue-to-digital converter and then passes an output signal of the amplifier on to a measurement circuit comprising a second analogue-to-digital converter supplying a second supplementary digital signal, as a result of which the accuracy of the converter circuit is increased, characterized in that the measurement circuit includes an integrator connected to the first switch, in that the second analogue-to-digital converter is connected to an output of the integrator, in that the first switch is closed during a constant period of time between two of the said conversion cycles and in that the second analogue-to-digital converter, when a given quantization level corresponding to a value which is at most equal to the value of the least significant bit of the first analogue-to-digital converter is exceeded, connects by means of a second switch a source to the input of the integrator in order to reset the output signal of the integrator with the said level, while further provision is made of a digital adder circuit having a first input for the first digital signal, a second input for the second digital signal and an output supplying the desired digital signal.

2. An analogue-to-digital converter circuit as claimed in Claim 1, characterized in that the second analogue-to-digital converter is a threshold value detector which has a threshold value equal to the said quantization level corresponding to the least significant bit of the first analogue-to-digital converter and which, when this level is exceeded by the output signal of the integrator, supplies a -1- signal as a second digital signal, which signal further keeps the second switch closed for a constant period of time, the said source supplying current, while the first digital signal is varied by one least significant bit.

3. An analogue-to-digital converter circuit as claimed in Claim 1, characterized in that the second analogue-to-digital converter is of the parallel type and in that a gate circuit is connected to the digital outputs of the second analogue-to-digital converter, which gate circuit determines the quantization level and supplies a signal when this level is exceeded for closing the second switch for a constant period of time, the said source supplying current.

4. An analogue-to-digital converter circuit as claimed in Claim 1 or 2, characterized in that the said source is a second digital-to-analogue converter, which is connected by its inputs to the second digital signal.



Patentansprüche

1. Analog/Digital-Wandlerschaltung mit einem ersten Analog/Digital-Wandler, der eine Vergleichsschaltung enthält mit einem ersten Eingang für ein umzusetzendes analoges Signal und mit einem zweiten Eingang für ein analoges Referenzsignal aus einem ersten an einen Ausgang der Vergleichsschaltung angeschlossenen und ein erstes Digitalsignal erzeugenden Analog/Digital-Wandler, mit einem ebenfalls an den Ausgang angeschlossenen Verstärker und mit einem ersten Schalter, der nach einem Umsetzungszyklus im ersten Analog/Digital-Wandler ein Steuersignal empfängt und darauf ein Verstärkerausgangssignal an eine Meßschaltung liefert, die einen zweiten, ein zweites ergänzendes Digitalsignal erzeugenden Analog/Digital-Wandler enthält, wobei infolge des letztgenannten Signals die Genauigkeit der Wandlerschaltung erhöht wird, dadurch gekennzeichnet, daß die Meßschaltung einen mit dem ersten Schalter verbundenen Integrator enthält, daß der zweite Analog/Digital-Wandler an einen Integratorausgang angeschlossen ist, daß der erste Schalter für die Dauer einer konstanten Zeit zwischen zwei der Umsetzungszyklen geschlossen ist und daß, wenn ein vorgegebener Quantisierungspegel entsprechend einem Wert, der höchstens gleich dem Wert des Bits mit niedrigster Wertigkeit im ersten Analog/Digital-Wandler ist, überschritten wird, der zweite Analog/Digital-Wandler zum Rückstellen des Integratorausgangssignals um den genannten Pegel eine Quelle über einen zweiten Schalter mit dem Integratoreingang verbindet, wobei außerdem ein digitaler Addierer mit einem ersten Eingang für das erste Digitalsignal, einem zweiten Eingang für das zweite Digitalsignal und einem das gewünschte Digitalsignal liefernden Ausgang vorgesehen ist.

2. Analog/Digital-Wandlerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der zweite Analog/Digital-Wandler ein Schwellenwertdetektor ist, dessen Schwellenwert gleich dem Quantisierungspegel entsprechend dem Bit mit niedrigster Wertigkeit im ersten Analog/Digital-Wandler ist und dieser Detektor beim Überschreiten dieses Pegels durch das Integratorausgangssignal ein -1- Signal als zweites Digitalsignal liefert, das weiter den zweiten Schalter für die Dauer einer konstanten Zeit geschlossen hält, wobei die Quelle Strom liefert und das erste Digitalsignal um wenigstens ein Bit mit niedrigster Wertigkeit variiert wird.

3. Analog/Digital-Wandlerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der zweite Analog/Digital-Wandler vom parallelen Typ ist, und daß eine Torschaltung mit den digitalen Ausgängen des zweiten Analog/Digital-Wandlers verbunden ist, die Torschaltung den Quantisierungspegel bestimmt und ein Signal erzeugt, wenn dieser Pegel zum Schließen des zweiten Schalters für die Dauer einer konstanten Zeit überschritten wird, wobei die Quelle Strom liefert.

4. Analog/Digital-Wandlerschaltung nach

Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Quelle ein zweiter Analog/Digital-Wandler ist, der durch seine Eingänge mit dem zweiten Digitalsignal verbunden ist.

Revendications

1. Circuit convertisseur analogique-numérique comprenant un premier convertisseur analogique-numérique comportant un circuit de comparaison pourvu d'une première entrée pour un signal analogique à convertir et d'une seconde entrée pour un signal de référence analogique provenant d'un premier convertisseur numérique-analogique, connecté à une sortie du circuit de comparaison et fournissant un premier signal numérique, un amplificateur également connecté à ladite sortie et un premier interrupteur qui reçoit un signal de commande après un cycle de conversion du premier convertisseur analogique-numérique et passe alors un signal de sortie de l'amplificateur à un circuit de mesure comprenant un second convertisseur analogique-numérique qui fournit un second signal numérique supplémentaire, ce qui a pour résultat d'augmenter la précision du circuit convertisseur, caractérisé en ce que le circuit de mesure comprend un intégrateur connecté au premier interrupteur, en ce que le second convertisseur analogique-numérique est connecté à une sortie de l'intégrateur, en ce que le premier interrupteur est fermé pendant une période constante entre deux desdits cycles de conversion et en ce que le second convertisseur analogique-numérique, lorsqu'un niveau de quantification donné correspondant à une valeur qui est tout au plus égale à la valeur du bit de plus faible poids du premier convertisseur analogique-numérique est dépassé, connecte, au moyen d'un second interrupteur, une source à l'entrée de l'intégrateur afin de ramener le signal de sortie de l'intégrateur à son état initial audit niveau tandis qu'est, en outre, prévu un circuit additionneur numérique comportant une première entrée pour le premier signal numérique, une seconde entrée pour le second signal numérique et une sortie fournissant le signal numérique souhaité.

2. Circuit convertisseur analogique-numérique suivant la revendication 1, caractérisé en ce que le second convertisseur analogique-numérique est un détecteur de valeur de seuil qui présente une valeur de seuil égale audit niveau de quantification correspondant au bit de plus faible poids du premier convertisseur analogique-numérique et qui, lorsque ce niveau est dépassé par le signal de sortie de l'intégrateur, fournit un signal -1- à titre de second signal numérique, ce signal maintenant également le second interrupteur fermé pendant une période constante, la source fournissant du courant, tandis que le premier signal numérique est modifié d'un bit de plus faible poids.

3. Circuit convertisseur analogique-numérique suivant la revendication 1, caractérisé en ce que le second convertisseur analogique-numérique est du type parallèle et en ce qu'un circuit-porte est connecté aux sorties numériques du second



convertisseur analogique-numérique, ce circuit-
porte déterminant le niveau de quantification et
fournissant un signal lorsque ce niveau est
dépassé, pour fermer le second interrupteur pen-
dant une période constante, la source fournissant
du courant.

4. Circuit convertisseur analogique-numérique
suivant la revendication 1 ou 2, caractérisé en ce
que la source est un second convertisseur nume-
rique-analogique qui est connecté par ses entrées
au second signal numérique.

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