

MEMORY CONTROLLER WITH QUEUE AND SNOOP TABLES

ABSTRACT

A memory controller (43) having request queue (52) and snoop tables (54) is provided for functioning with bus interface units (38, 40, 42, 44) interposed between a multiple processor bus (48) and individually coupled to the respective processors (22, 24, 26, 28) in a complex incorporating a multitude of processors, where each bus interface unit includes block snoop control registers responsive to signals from a system memory controller including enhanced function supportive of I/O devices (45) with and without block snooping compatibility. The tables are compared to minimize and more efficiently institute snoop operations as a function of the presence or absence of the same listings in the tables. The BIU provides functionality for the bus of the multiple processors to be processor independent. This architecture reduces the number of snoop cycles which must access the processor bus, thereby effectively increasing the available processor bus bandwidth. This in turn effectively increases overall system performance.

Fig. 5