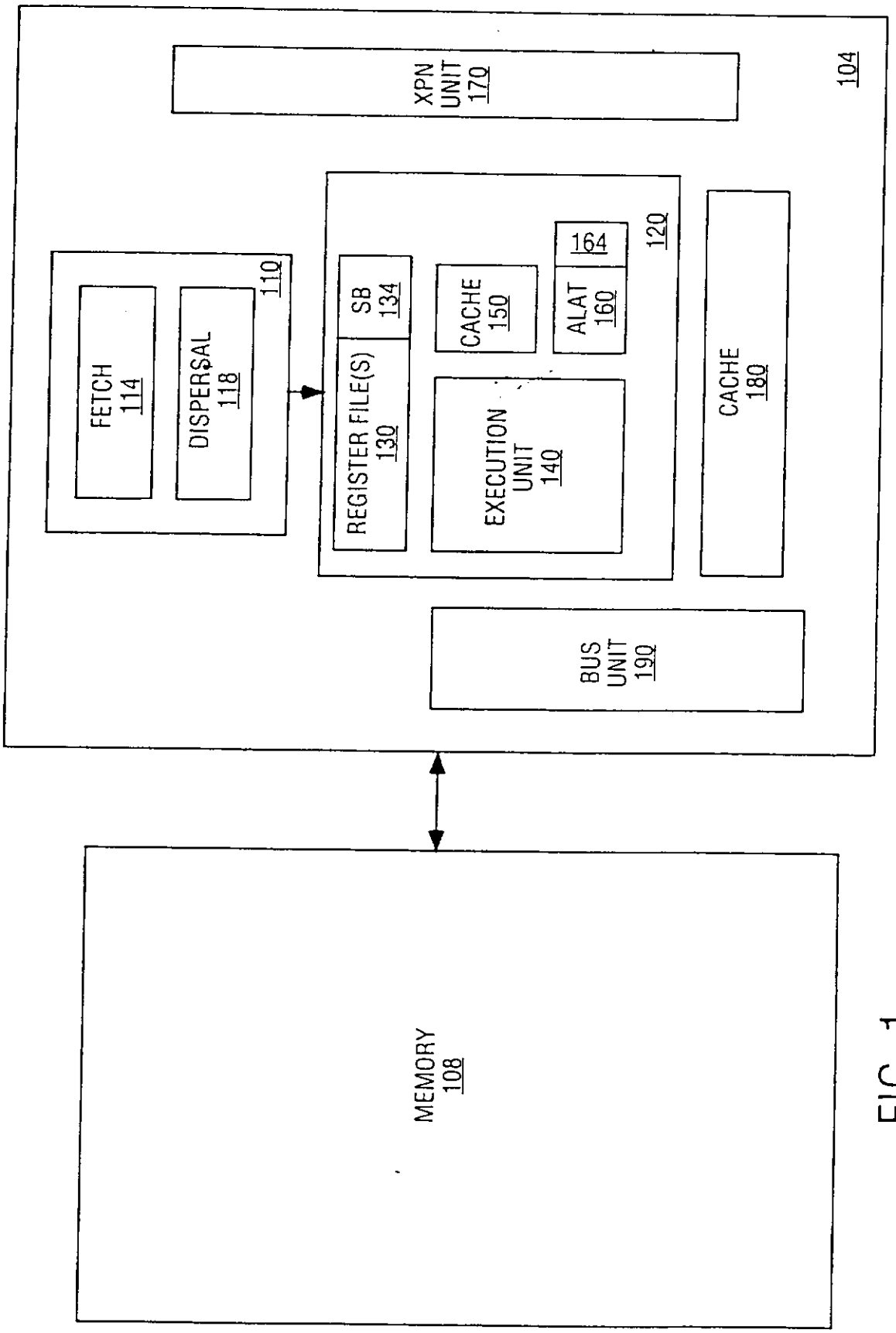

XPN UNIT 170
104
FETCH 114
DISPERSAL 118
110
REGISTER FILE(S) 130
SB 134
CACHE 150
ALAT 160
164
120
EXECUTION UNIT 140
CACHE 180
BUS UNIT 190
MEMORY 108

FIG. 1

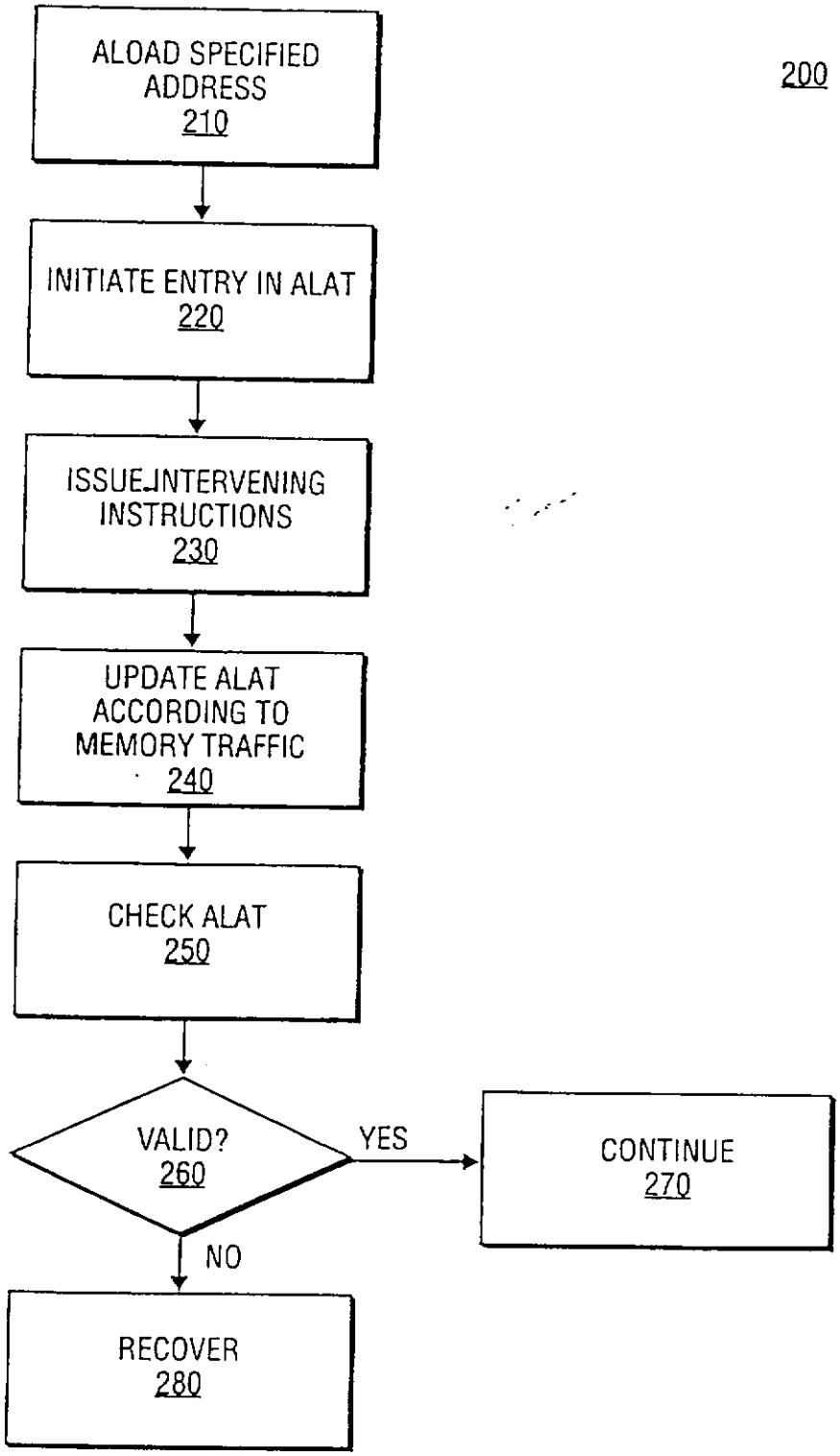

ALOAD SPECIFIED ADDRESS 210
200
INITIATE ENTRY IN ALAT 220
ISSUE_INTERVENING INSTRUCTIONS 230
UPDATE ALAT ACCORDING TO MEMORY TRAFFIC 240
CHECK ALAT 250
VALID? 260
YES
CONTINUE 270
NO
RECOVER 280

FIG. 2

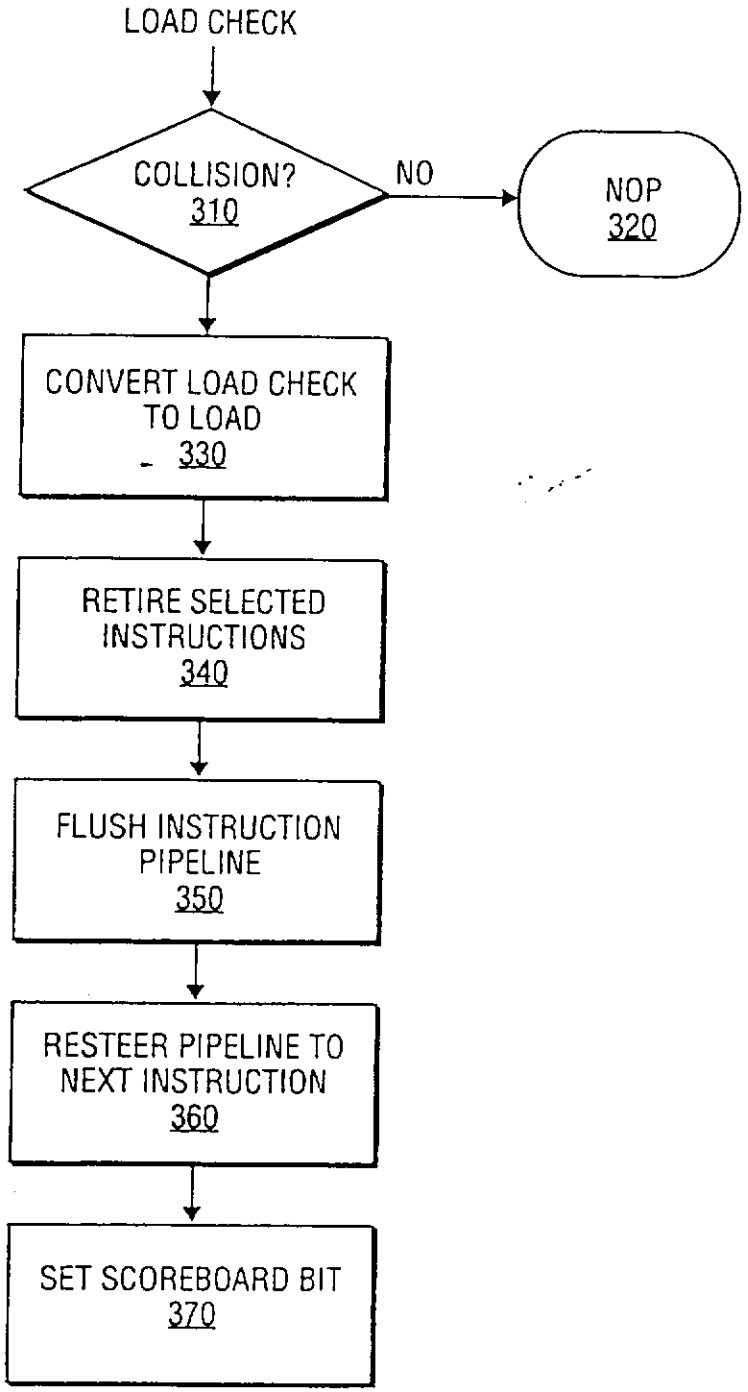

LOAD CHECK
COLLISION?
310
NO
NOP
320
CONVERT LOAD CHECK TO LOAD
330
RETIRE SELECTED INSTRUCTIONS
340
FLUSH INSTRUCTION PIPELINE
350
RESTEER PIPELINE TO NEXT INSTRUCTION
360
SET SCOREBOARD BIT
370

FIG. 3

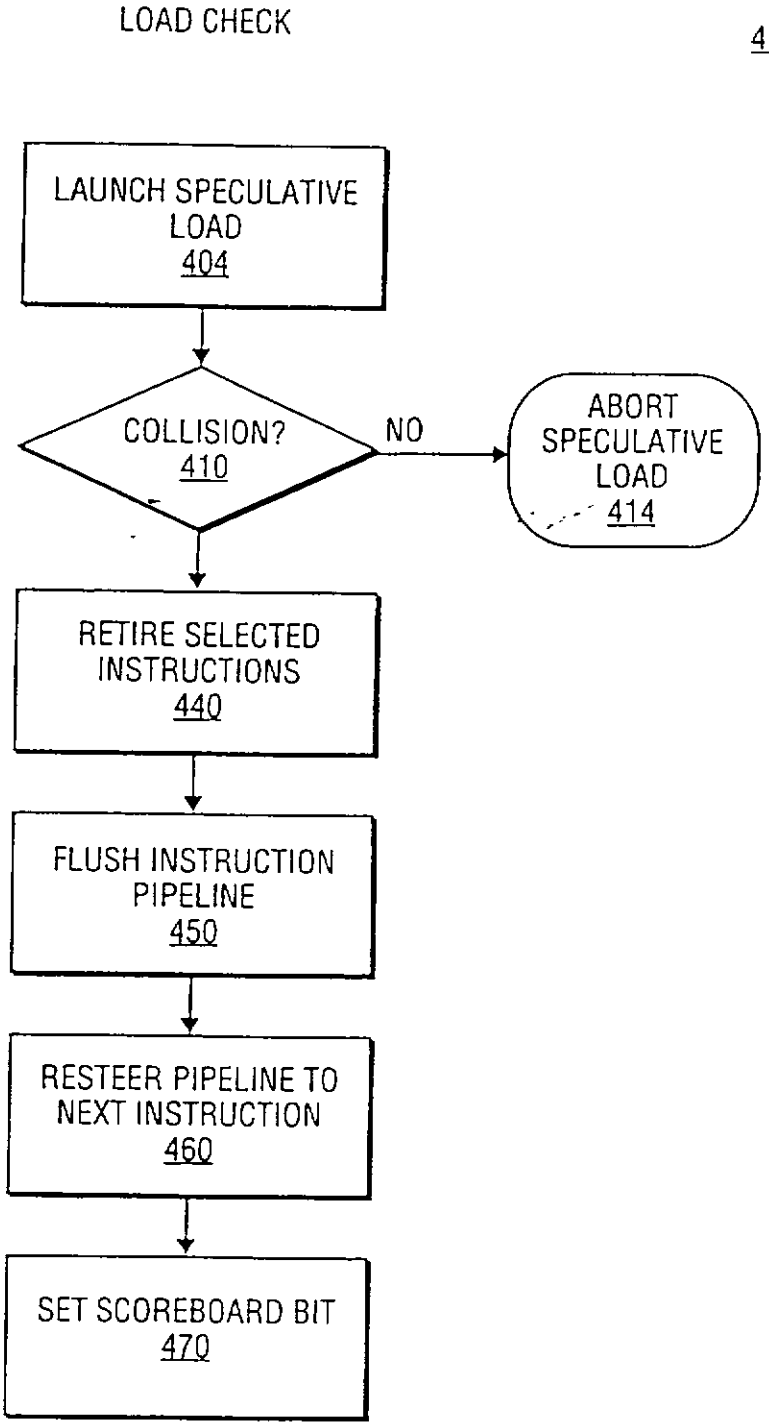

LOAD CHECK
400
LAUNCH SPECULATIVE LOAD
404
COLLISION?
410
NO
ABORT SPECULATIVE LOAD
414
RETIRE SELECTED INSTRUCTIONS
440
FLUSH INSTRUCTION PIPELINE
450
RESTEER PIPELINE TO NEXT INSTRUCTION
460
SET SCOREBOARD BIT
470

FIG. 4

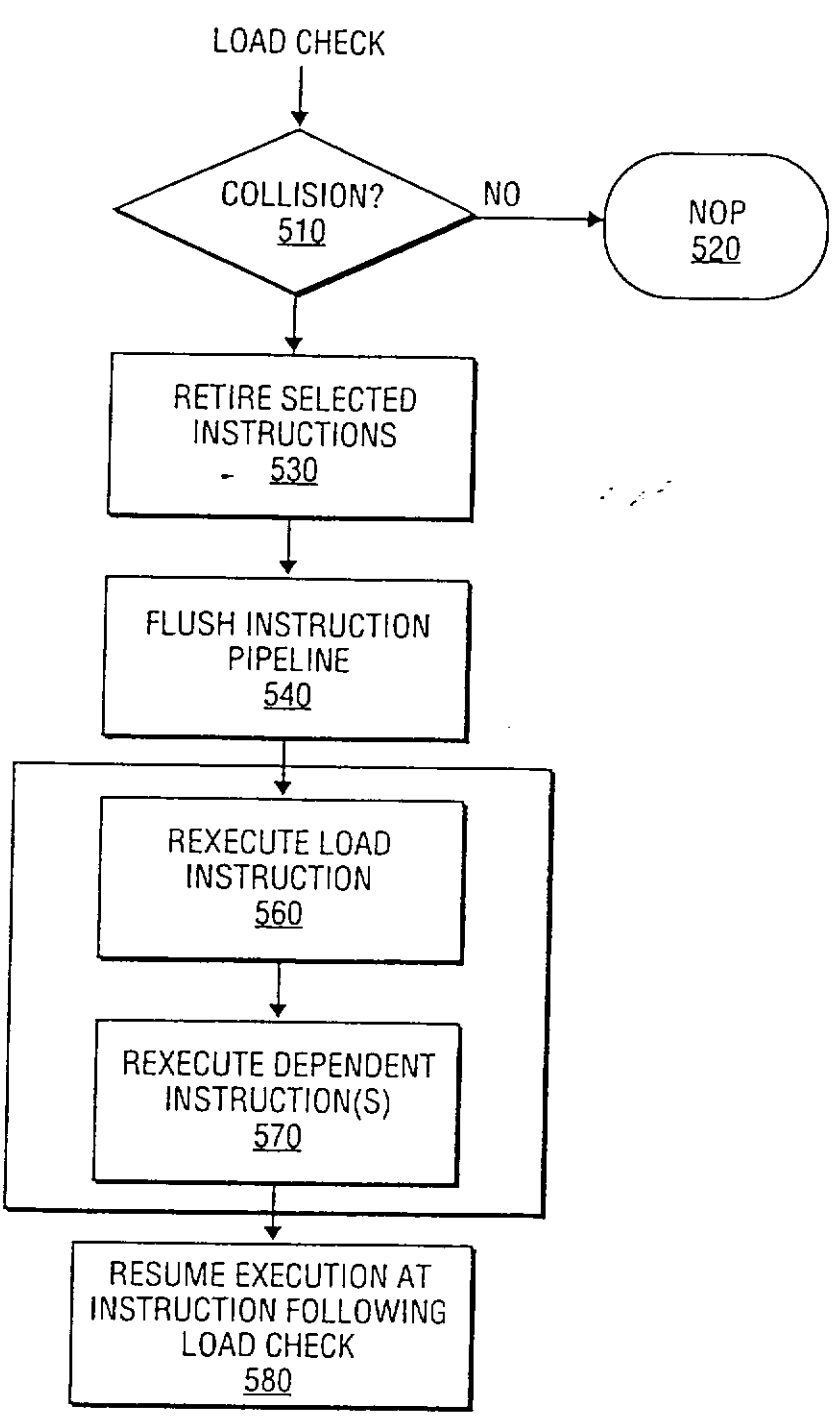

500
LOAD CHECK
COLLISION?
510
NO
NOP
520
RETIRE SELECTED
INSTRUCTIONS
530
FLUSH INSTRUCTION
PIPELINE
540
REXECUTE LOAD
INSTRUCTION
560
REXECUTE DEPENDENT
INSTRUCTION(S)
570
RESUME EXECUTION AT
INSTRUCTION FOLLOWING
LOAD CHECK
580

FIG. 5

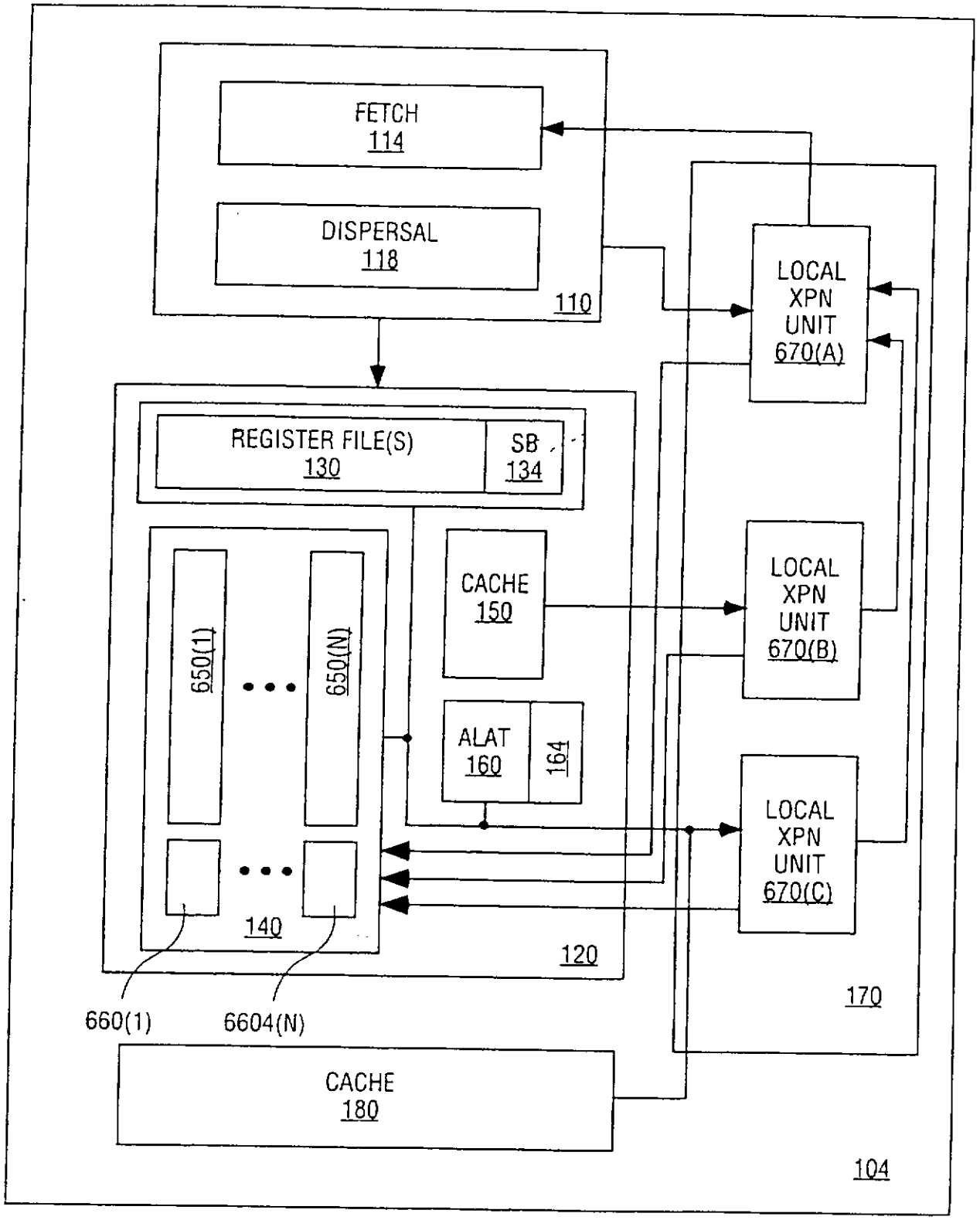

FETCH
114
DISPERSAL
118
110
LOCAL
XPN
UNIT
670(A)
REGISTER FILE(S)
130
SB
134
CACHE
150
LOCAL
XPN
UNIT
670(B)
650(1)
650(N)
ALAT
160
164
LOCAL
XPN
UNIT
670(C)
140
120
170
660(1)
6604(N)
CACHE
180
104

FIG. 6

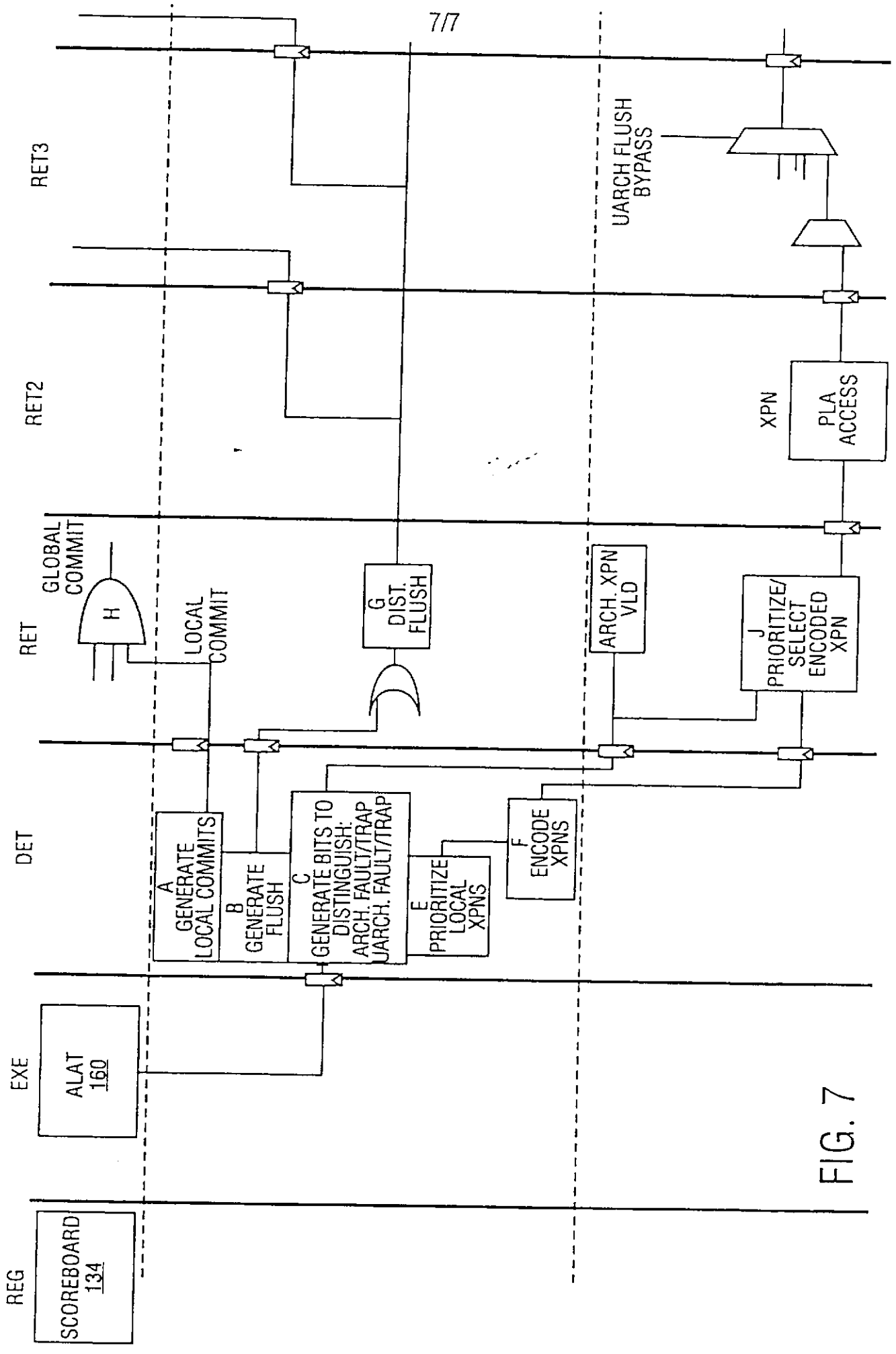

RET3
RET2
RET
DET
EXE
REG
UARCH FLUSH BYPASS
XPN
PLA ACCESS
GLOBAL COMMIT
H
LOCAL COMMIT
G DIST. FLUSH
ARCH. XPN VLD
J PRIORITIZE/ SELECT ENCODED XPN
A GENERATE LOCAL COMMITS
B GENERATE FLUSH
C GENERATE BITS TO DISTINGUISH: ARCH. FAULT/TRAP UARCH. FAULT/TRAP
E PRIORITIZE LOCAL XPNS
F ENCODE XPNS
ALAT 160
SCOREBOARD 134

FIG. 7