

PROCESSOR ASSEMBLY, QUANTUM COMPUTING ARRANGEMENT AND METHOD

FIELD OF THE DISCLOSURE

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This disclosure relates to quantum computing, and more particularly to cooling quantum processor units (QPUs). The present disclosure further concerns electrical connections to QPUs.

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BACKGROUND OF THE DISCLOSURE

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Many quantum computers contain quantum processing units (QPUs) that have to be operated at millikelvin temperatures, for example in a cryostat. There is typically a temperature gradient inside a cryostat. It contains multiple cooling stages with different temperatures. The temperature at four successive stages of a cryostat may for example be on the order of 10^1K , 10^0K , 10^{-1}K and 10^{-2}K . The QPUs are placed at the lowest temperature stage.

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Complex electric circuitry is needed to facilitate signal transfer to and from a QPU. Distributing the required electric circuitry inside the cryostat is a complex engineering problem because the layout needs to be optimized both from a thermal and from an electrical perspective (other considerations, such as limited space, add even more complexity). If a circuit component placed at a given temperature stage would emit too much heat, then too much cooling power may be needed for achieving the target temperature at this temperature stage. The remaining cooling power might then be insufficient for reaching the target temperature of the subsequent (lower temperature) stages. These design problems become particularly challenging with large QPUs that contain hundreds of quantum bits, and thousands of signal lines and flux lines.

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QPUs are typically not installed permanently inside a cryostat. Instead, the QPUs are built on a removable processor assembly which can be installed in the cryostat for use and then removed from the cryostat after use.

Two kinds of connections need to be established between a processor assembly and the cryostat when the assembly is installed. The first is an electrical connection. The inside of

a cryostat contains fixed cryostat cabling which is used to transmit signals to and from the QPU when the quantum computer is used. When a processor assembly is installed in the cryostat, an electric connector on the removable processor assembly is typically connected to a corresponding electrical connector in the cryostat cabling. The QPUs are thereby
5 electrically connected to the outside world. Secondly, a thermal connection must be made to the lowest temperature stage. This thermal connection can be established by mounting the processor assembly onto a cold plate in the cryostat with a mechanical connection which has good heat conductivity.

10 It is known that a processor assembly can be mounted inside a cryostat with a single thermal connection to a cold plate. The entirety of the processor assembly, including the electrical connectors, will then be brought to the temperature of that cold plate. A general problem with this arrangement is that, when the quantum computer is used, Joule heating always takes place at the electrical interface between the electric connector on the removable processor assembly and the electrical connector on the cryostat cabling.

15 The target temperature of the lowest temperature stage is typically 20mK or less in quantum computing applications. The size (number of qubits) of the largest QPU that can be installed in a cryostat is always limited by the available cooling power. One of the main limitations in the prior art is that the heat generated at electrical interfaces is released at the lowest temperature stage. In other words, the size of the QPU must be kept small
20 because too much heat would be generated if the number were to be increased.

One way to address the problem would be to decrease Joule heating at electrical interfaces by decreasing contact resistance at these interfaces. A smaller current density could for example be achieved by enlarging the physical dimensions of the conductors which form interface. But this is not a practical solution because large processor
25 assemblies may contain hundreds or thousands of interfaces, and they would consume too much space inside the cryostat if all of them would be enlarged.

BRIEF DESCRIPTION OF THE DISCLOSURE

30 An object of the present disclosure is to provide an apparatus for alleviating the above dilemma. The object of the disclosure is achieved by an arrangement which is characterized by what is stated in the independent claim. The preferred embodiments of the disclosure are disclosed in the dependent claims. The disclosure is based on the idea

of implementing a temperature gradient inside the processor assembly and coupling electrical connectors to a higher temperature stage.

BRIEF DESCRIPTION OF THE DRAWINGS

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In the following the disclosure will be described in greater detail by means of preferred embodiments with reference to the accompanying drawings, in which

Figure 1 illustrates three symbols that are utilized in this disclosure.

Figures 2a – 2b and 2e – 2f illustrate processor assemblies.

10 Figures 2c – 2d illustrate wiring boards with an electrical signal connection.

Figure 3 illustrates a quantum computing arrangement.

Figures 4a – 4d illustrate quantum computing arrangements with a magnetic shielding enclosure.

15 Figures 5a – 5c also illustrate quantum computing arrangements with a magnetic shielding enclosure.

Figures 5d and 5e illustrate arrangements for bringing an electrical connector outside of a magnetic shielding enclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

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This disclosure describes a processor assembly for a quantum computer. The assembly comprises a carrier and at least one quantum processor die mounted on the carrier. The assembly also comprises a first thermal anchor point which is in thermal contact with the carrier. The assembly also comprises a first electrical connector and an electrical signal connection which comprises a first end which is electrically connected to the carrier and a second end which is electrically connected to the first electrical connector. The processor assembly also comprises a second thermal anchor point. The second thermal anchor point is thermally separated from the first thermal anchor point. The second thermal anchor point is in thermal contact with the first electrical connector.

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The term “processor assembly” refers in this disclosure to a structure which holds a quantum processor die and can be removably mounted inside a cryostat. The processor assembly may also be called a sample box or sample holder, and the quantum processor die may be called a sample. The processor assembly may in some embodiments be called a plug-in processor assembly, a releasable processor assembly or a connectorized processor assembly.

The term “electrical connector” refers to an electrical component which forms the end of an electrical line. The electrical connector comprises connection structures which allow the connector to be releasably attached to another electrical connector. In this disclosure, the electrical connector in the processor assembly is called the first electrical connector. It forms a part of the processor assembly, so it is transferred to the cryostat together with the processor assembly.

The counterpart to the first electrical connector is called the second electrical connector in this disclosure. The second electrical connector is built inside the cryostat, and it forms a part of the fixed cabling in the cryostat. When the processor assembly is placed inside the cryostat, the first and second electrical connectors are connected to each other. This connects the processor assembly electrically to the outside world.

The first and second electrical connectors may be plug-in connectors, or any other releasable connector type. One of the connectors may be male type and the other female type. The connectors may comprise a locking mechanism which keeps the first and second electrical connectors firmly attached to each other. They may also comprise a button, or some other mechanism, which is configured to open the locking mechanism when the button is pushed. This allows them to be easily released from each other when the processor assembly is removed from the cryostat.

The at least one quantum processor die may be mounted on the carrier. The carrier may also be called a sample holder. The carrier may comprise a printed circuit board (PCB) where the QPU die is mounted. The circuit board may for example be made of a ceramic material, FR4, polyimide or any other suitable PCB material. Throughout this disclosure, any electrical connection which is made to the carrier may be an electrical connection to a quantum processor die on the carrier.

The first and second thermal anchor points are structures with good heat conductivity. They may for example be blocks of metal. The thermal anchor points described in this disclosure may also be called anchor blocks. The thermal anchor points can for example be made of copper, and they may optionally be coated with gold. The thermal anchor

points may be rigid mechanical structures which provide structural integrity to the processor assembly and support the weight of the other parts in the assembly.

The detailed design of the mechanical structures in the processor assembly will depend on how the processor assembly is attached to the cryostat. A variety of attachment means could be used. The figures of this disclosure which lack coordinate axes are schematic figures which do not illustrate the relative positions of the parts in the processor assembly and the cryostat in the real world. Instead, they merely illustrate connections between these parts with symbols.

Figure 1 explains three key symbols utilized in this disclosure. A white arrow 11 is used to illustrate an electrical connection between two parts. This connection may comprise electrical conductors where electrical signals can be transmitted from one part to another. A black arrow 12 illustrates a thermal connection between two parts. This connection comprises a thermal conductor which allows heat to be effectively transmitted from one part to another. Finally, a grey arrow 13 illustrates a mechanical connection between two parts. This connection comprises a rigid structure which connects the two parts to each other and keeps them in fixed positions in relation to each other.

As described in more detail below, both the electrical connections 11 and the mechanical connections 13 described in this disclosure have low heat conductivity. In other words, very little heat transmission occurs via the connections illustrated with arrows 11 and 13. In some cases, the electrical and mechanical connections can be implemented together, as described below with reference to figures 2c and 2d. The illustrated connections 11 – 13 can in practice be implemented in many different parts. Some preferred possibilities will be discussed below.

Figure 2a illustrates a processor assembly 20 with a carrier 21 and a quantum processor die 29 on the carrier 21. The assembly comprises a first thermal anchor point 221 which is in thermal contact with the carrier 21. The carrier 21 may for example be mounted on the first thermal anchor point 221 so that there is direct mechanical contact between the carrier 21 and the first thermal anchor point 221. The carrier 21, and the quantum processor die 29 on the carrier 21, may be at the same temperature as the first thermal anchor point 221. The first thermal anchor point 221 may surround a part of the carrier 21.

The processor assembly 20 also comprises an electrical signal connection 24 which has a first end 241 and a second end 242. The first end 241 of the electrical signal connection 24 is electrically connected to the carrier 21. Furthermore, the first end 241 of the electrical

signal connection 24 may be connected to the quantum processor die 29 via conductors and/or electrical leads in the carrier 21.

The second end 242 of the electrical signal connection 24 is electrically connected to a first electrical connector 25. The first electrical connector 25 is also thermally connected to a second thermal anchor point 222. The first electrical connector 25 may for example be mounted on the second thermal anchor point 222 so that there is direct mechanical contact between the first electrical connector and the second thermal anchor point 222.

In figure 2a the first end 241 is in thermal contact with the first thermal anchor point 221. This thermal connection can be implemented for example by gluing a part of the first end 241 to the first thermal anchor point 221 with a dielectric glue which has high thermal conductance. The first end 241 may still be electrically connected directly to the carrier 21, as figure 2a illustrates.

The same connection can be implemented between the second end 242 of the electrical signal connection 24 and the electrical connector 25. All options discussed in the previous paragraph apply here also. Figure 2a illustrates a thermal connection between the second end 242 of the electrical signal connection 42 and the second thermal anchor point 222.

The second end 242 of the electrical signal connection 24 may in practice extend all the way to the first electrical connector, even though they are illustrated apart from each other in figure 2a. The same applies to the first end 241 of the electrical signal connection 24, which may extend all the way to the carrier 21. The electrical signal connection 24 is illustrated just as a single box in figure 2a. Nevertheless, this signal connection may for example comprise a cable or wire which functions as each of the electrical connections 11 and each of the thermal connections 12 illustrated in figure 2a. These considerations apply to all embodiments presented in this disclosure, and also to any additional electrical signal connections in the processor assembly, such as connection 27 in figures 2e and 2f. More generally, the symbols presented in figure 1 are used in the figures of this disclosure to illustrate the functions performed by other elements in the same figure.

The electrical interface between the first electrical connector 25 and a second electrical connector (not illustrated in figure 2a) will emit heat when the processor assembly is used in the cryostat. However, as described in more detail with reference to figure 3 below, the processor assembly illustrated in figure 2a (and the assemblies illustrated in the other figures of this disclosure) allows the first electrical connector 25 and the carrier 21 to be thermally connected to different temperature stages in the cryostat. The first thermal anchor point 221 can be connected to the lowest temperature stage, so that the quantum

processor die 29 will reach its target temperature. But the second thermal anchor point 222 can be connected to a higher temperature stage (which may, but does not necessarily have to, be the second lowest stage).

5 In other words, the first electrical connector 25 may be placed at a higher temperature than the carrier 21 and the quantum processor die 29 when the device is being used. The heat generated at the connector is the same regardless of temperature. The higher the temperature stage, the more cooling power is available at that particular stage. Hence, thermalizing the connector to a higher temperature stage at the second thermal anchor point 222 (rather than the lower temperature stage at the first thermal anchor point 221) 10 saves cooling power. In other words, the cooling power budget can be relaxed by allowing the processor assembly 20 to tap into the cooling power of the high-temperature stage which is thermally connected to the second thermal anchor point 222.

The processor assembly may comprise more than one first electrical connectors and more than one quantum processor dies, all of which may be built into the processor assembly in the manner described above. When all first electrical connectors are connected to a higher 15 temperature stage than the quantum processor dies, the relaxation of the available cooling power budget can allow the number of qubits in the quantum computer to be increased.

Figure 2a illustrates the electrical signal connection 24 between the first and second thermal anchor points 221 and 222. It is evident from the above discussion that the 20 electrical signal connection 24 should not have high heat conductivity. The electrical signal connection 24 may be made of a superconducting material. The electrical interconnections between the first end 241 of the electrical signal connection 24 and the carrier 21 may also be made of superconducting materials. Heat-generation and heat conductivity is typically very low in superconducting materials.

25 Alternatively or complementarily, the heat conductivity of the electrical signal connection 24 may be lowered by increasing the length of the cables or signal lines or conductors which form this connection.

In any embodiment presented in this disclosure, the superconducting material in the electrical signal connection may for example be a metallic element such as Ti, Mo, Al, Nb, 30 Re or In. Alternatively, it may be an alloy such as NbN, TiN, NbTiN or a compound such as the ReBCO family.

Many considerations may influence the selection of the superconducting material. The critical temperature of the material should be higher than the final operating temperature of the electrical signal connection. Its supercurrent density should be sufficiently high. Its

residual electronic heat leak should also be sufficiently low, since the electrical signal connection supports a significant thermal gradient. In addition, metallurgical aspects such as solderability and chemical stability may also have to be considered.

5 Optionally, the first thermal anchor point 221 may be mechanically connected to the second thermal anchor point 222 with a mechanical interconnector 28 which maintains the structural integrity of the processor assembly 20. This has been illustrated in figure 2b. The electrical signal connection 24 may be flexible, but the mechanical interconnector 28 may be rigid. The processor assembly may be easier to handle if the first and second thermal anchor points 221 and 222 are locked to a fixed relative position in this manner. The
10 optional mechanical interconnector 28 must have low thermal conductivity because it should not form a thermal connection between the first and second thermal anchor points 221 and 222 that are to be held at different temperatures. The conducting parts in the mechanical interconnector 28 may be made of steel, for example austenitic stainless steel. The mechanical interconnector may comprise casing. The casing may be insulating, and
15 it may comprise fiberglass–epoxy composites, polyimide, phenolic resins, ceramics or glass. One or more mechanical interconnectors with low thermal conductivity may be implemented in any embodiment presented in this disclosure.

20 The electrical signal connection 24 may comprise a coaxial cable. If multiple electrical signal connections are connected to the carrier 21, then each signal connection may be a coaxial cable. A first electrical connector 25 may be connected to the second end of each coaxial cable. The core of the coaxial cable may be superconducting. The outer conductor of the coaxial cable may also be superconducting.

25 Alternatively, the electrical signal connection may comprise a wiring board which has a main surface. The electrical signal connection may comprise a conductor which is in the wiring board and extends substantially parallel to the main surface of the wiring board.

30 This is illustrated in figure 2c, which shows a wiring board 27 which extends from the first thermal anchor point 221 to the second thermal anchor point 222 in the direction of a y-axis. This figure is not purely schematic. The x and y coordinate axes refer to directions in the real world, but the parts have not been drawn to scale. An electrical conductor 240, which forms the electrical signal connection 24, has been formed in the wiring board 27.

In any embodiment presented in this disclosure, a wiring board which is used to support the electrical signal connection 24 may for example be made of a ceramic package, or a silicon wafer or sapphire wafer. Other dielectric wafers may also be used.

The wiring board 27 has a main surface (either 278 or 279). The main surface may for example be the surface of the circuit board which has the largest surface area. The width of the wiring board 27 in the illustrated x-direction may be much less than its height in the illustrated y-direction. The electrical conductor 240 may for example be a trace of conductive material. The electrical conductor 240 may be inside the wiring board 240, as figure 2c illustrates, or on the surface of the wiring board 27. In practice, the wiring board may comprise multiple conductors (not illustrated) which extend in the y-direction. Some of these multiple conductors may be grounded, while others are used for signal transmission. One or more grounded conductors may be on the surfaces (278, 279) of the wiring board 27, while one or more signal transmission lines such as 240 may be inside the wiring board 27. Optionally, the conductive material in any electrical conductor mentioned above may be superconducting.

The one or more wiring boards may in this configuration also be used as the mechanical interconnector (illustrated as 28 in figure 2b) which forms a rigid mechanical connection between the two thermal anchor points 221 and 222. Multiple wiring boards could alternatively be stacked upon each other.

Figure 2d illustrates another alternative where the electrical signal connection comprises a wiring board 275, and the wiring board has a main surface, and the electrical signal connection comprises a conductor 240 which is in the wiring board 275 and extends substantially orthogonally to the main surface of the wiring board 275.

The main surface of the wiring board 275 may in this case be the upper (larger y-coordinate) or lower (smaller y-coordinate) surface of the wiring board 275. Again, the main surface may for example be the surface of the circuit board 275 which has the largest surface area. The width of the wiring board 275 in the illustrated x-direction may be much greater than its height in the illustrated y-direction.

Multiple wiring boards may be used. Three stacked wiring boards 275 – 277 are illustrated, but only one wiring board could alternatively be used. The conductor 240 may in this case comprise electrically conductive vias which extend through each wiring board 275, 276 and 277. The wiring boards 275 – 277 may be stacked upon each other so that the vias are aligned in the y-direction, the vias form the electrical signal connection 24 through the stack. The vias may be joined electrically to each other by using solder or indium, for example in the form of bumps or balls that get crushed or re-flown during assembly. Electrically conductive glue may alternatively be used to join the vias electrically to each other. The vias may be slightly staggered so that they have different x-coordinates.

As in figure 2c, the one or more wiring boards 275 – 276 may optionally also be used as the mechanical interconnector (illustrated as 28 in figure 2b) which forms a rigid mechanical connection between the two thermal anchor points 221 and 222. The conductor 240, and the electrically conductive vias which form the conductor, may optionally be made of a superconducting material.

Figure 2e and 2f illustrate a processor assembly which also one or more additional thermal anchor points 223 which are thermally separated from the first thermal anchor point 221, thermally separated from the second thermal anchor point 222 and thermally separated from each other.

The one or more additional thermal anchor points may for example comprise one, two or three additional thermal anchor points. The one or more additional thermal anchor points may be thermally connected to any additional element which is included in the processor assembly. This additional element may in any embodiment of this disclosure be a dissipative or non-linear signal-conditioning element.

Any option described above with reference to the thermal isolation between the first and the second anchor points is also applicable to

- the thermal isolation between the first and/or second anchor points and the one or more additional thermal anchor points, and
- the thermal isolation between the one or more additional thermal anchor points, if their number exceeds one.

Furthermore, the electrical connection between the carrier and the additional element, and/or between the carrier and the first electrical connector, may implemented for example in the same way as the electrical signal connection described above.

Figure 2e illustrates a processor assembly where an additional electrical signal connection 27 connects a dissipative or non-linear signal-conditioning element 26 to the carrier 21. The two electrical signal connections 24 and 27 are here parallel to each other. In other words, the electrical signal connection 24 and the additional electrical signal connection 27 are separately connected to the carrier 21.

Figure 2f illustrates an alternative configuration where the two electrical signal connections are connected in series. In other words, the electrical signal connection 24 is connected to the first electrical connector 25 via the dissipative or non-linear signal-conditioning element 26, the additional electrical signal connection.27 and the second thermal anchor point 222.

In both figures 2e and 2f, the three thermal anchor points may be connected to three different temperature stages in the cryostat. The parts of the processor assembly which are thermally connected to different thermal anchor points will thereby be held at different temperatures when the device is used. The processor assembly 20 can thereby tap into the cooling power of two different high-temperature stages which are thermally connected to the second and third thermal anchor points 222 – 223.

Mechanical connections such as 28 in figure 2b may also be implemented between any of the thermal anchor points 221 – 223 in figures 2e – 2f. This has not been illustrated.

As mentioned above, the number of additional thermal anchor points in the processor assembly may be greater than one. Correspondingly, more than one additional element, similar to the first electrical connector 25 and the dissipative or non-linear signal-conditioning element 26, may then be held at different temperatures in the processor assembly 20.

In any embodiment presented in this disclosure, the processor assembly may also comprise signal-conditioning circuitry (not illustrated) which is electrically coupled to some parts of the electrical signal connections described above. This signal-conditioning circuitry may be primarily reflective, inductive or capacitive, in which case Joule heating can be avoided in this circuitry. Separate signal-conditioning circuitry may be employed at different temperatures. In other words, there may be one set of signal-conditioning circuitry on the carrier, thermally connected to the first thermal anchor point, and other sets of signal-conditioning circuitry in the components that are connected to the second and third thermal anchor points.

Any processor assembly described in this disclosure may form a part of a quantum computing arrangement. In other words, a quantum computing arrangement may comprise any of the processor assemblies described in this disclosure.

Figure 3 illustrates a quantum computing arrangement 30. Reference numbers 21, 24, 29, 221 and 222 indicate the parts of the processor assembly that were introduced in figures 2a – 2f above. The schematic representation of the processor assembly in figure 3 (and figures 4a – 4d below) corresponds to that of figure 2a. However, any of the other schemes shown in figures 2a – 2f could equally well be used in the arrangement 30.

In addition to the processor assembly, the quantum computing arrangement in figure 3 may comprise the following parts:

- A cryogenic vacuum chamber 31. The processor assembly is inside the cryogenic vacuum chamber 31.
- A fixed cable connection 36 which is inside the cryogenic vacuum chamber 31. The fixed cable connection 36 comprises a second electrical connector 35. The second electrical connector 35 is electrically connected to the first connector 25 of the processor assembly. These two connectors are therefore illustrated in a single box marked 25 & 35.
- A first cold plate 321 and a second cold plate 322 which are inside the cryogenic vacuum chamber 31. The temperature of the first cold plate 321 is lower than the temperature of the second cold plate 322.

The first cold plate 321 is in thermal contact with the first thermal anchor point 221 in the processor assembly. The second cold plate 322 is in thermal contact with the second thermal anchor point 222 in the processor assembly.

The cold plates may be structures with high heat conductivity which are configured to be set to specific temperatures given temperature when the cryostat is operated. The cold plates can for example be made of copper, and they may optionally be coated with gold. The cold plates may be rigid mechanical structures which support the weight of the processor assembly when the assembly is installed in the cryostat. However, the first and second cold plates may be different in this regard. One of the cold plates may be a rigid mechanical structure which provides a fixed point of support, while the other may be a flexible structure which provides a heat-conduction path but not structural support.

The first and second cold plates may be coupled to different temperature stages. The first cold plate may be set to a lower temperature than the second cold plate. The first cold plate may be refrigerated to the lowest temperature stage. The second cold plate may, but does not have to be, refrigerated to the second lowest temperature stage. The second cold plate could alternatively be set to a higher temperature stage.

The thermal contact between each cold plate and the corresponding thermal anchor point may be implemented with a mechanical structure which also provides mechanical support for the processor. This mechanical structure may fix the processor assembly releasably to the interior of the cryostat 31. The mechanical connection has been illustrated with arrows in figure 3.

The fixed cable connection 36 in the cryostat 31 may comprise filters, attenuators, amplifiers and passive microwave components. The fixed cable connection may be electrically connected to an external electrical circuit 38. When the quantum computing arrangement 30 is used, the external circuit 38 may be configured to send and retrieve signals to and from the quantum processor die 29.

The quantum computing arrangement may also comprise a magnetic-shielding enclosure which at least partly surrounds the processor assembly. The magnetic shielding enclosure may alternatively surround the processor assembly on all sides.

Figure 4a illustrates schematically a magnetic shielding enclosure 41 in the quantum computing arrangement 31. The magnetic shielding enclosure 41 is inside the cryostat 31.

The magnetic shielding enclosure 41 may for example comprise a first part (not separately illustrated) which is installed in the cryostat 31 and is not removed from the cryostat when the processor assembly is removed from the cryostat. The magnetic shielding enclosure 41 may then also comprise a second part (not illustrated) which is attached to the processor assembly and removed from the cryostat when (or before) the processor assembly is removed from the cryostat 31.

The first part of the magnetic shielding enclosure 41 may form a part of the mounting structure in the cryostat 31 where the processor assembly can be mounted. The cold plates 321 – 322 may form parts of the same mounting structure. The processor assembly may then be partly or fully surrounded by the magnetic shielding enclosure when both the processor assembly and the second part of the magnetic shielding enclosure have been mounted in cryostat 31. Other options are also possible.

The interface between the first and second electrical connectors, illustrated as box 25 & 35 in figure 4a, may be located inside the magnetic shielding enclosure 41 as figure 4a illustrates.

Figure 4a illustrates an embodiment where the first and second thermal anchor points 221 and 222 are located inside the magnetic shielding enclosure 41 and the first and second cold plates 321 – 322 are located outside of the magnetic shielding enclosure. The thermal and mechanical connections 481 and 482 between the thermal anchor points 221 – 222 and the cold plates 321 – 322 may in this case comprise thermal and mechanical linkages which extend from the inside of the magnetic shielding enclosure 41 to the outside of the magnetic shielding enclosure 41, as figure 4a illustrates schematically. These thermal and mechanical linkages may form a part of the processor assembly and they may be

releasably connected to the first and second cold plates 321 – 322 when the processor assembly is mounted into the cryostat 31.

Other options are also possible. The first and second thermal anchor points 221 and 222 could for example extend from the inside of the magnetic shielding enclosure 41 to the outside of the magnetic shielding enclosure 41.

Figure 4b illustrates an embodiment where the first cold plate 321 extends from the outside of the magnetic shielding enclosure 41 to the inside of the magnetic shielding enclosure 41. The thermal and mechanical connection 481 between the first cold plate 321 and the first thermal anchor point 221 therefore lies inside the magnetic shielding enclosure 41. On the other hand, the thermal and mechanical connection 482 between the second cold plate 322 and the second thermal anchor point 222 extends through the magnetic shielding enclosure 41, as in figure 4b.

Figure 4c illustrates an embodiment where the first cold plate 321 is located outside of the magnetic shielding enclosure 41 and the first thermal anchor point 221 is located inside the magnetic shielding enclosure 41. The first thermal anchor point 221 is thermally and mechanically connected to a first thermal and mechanical linkage 481 inside the magnetic shielding enclosure 41. The first thermal and mechanical linkage 481 extends from the inside of the magnetic shielding enclosure 41 to the outside of the magnetic shielding enclosure 41. The thermal and mechanical linkage 481 is thermally and mechanically connected to the first cold plate 321 outside of the magnetic shielding enclosure 41.

In figure 4c the second cold plate 322 extends from the outside of the magnetic shielding enclosure 41 to the inside of the magnetic shielding enclosure 41. The second thermal anchor point 222 is thermally connected to the second cold plate 322 inside the magnetic shielding enclosure 41 with a second thermal and mechanical linkage 482.

Other combinations are also possible. One or both of the first and second cold plates 321 – 322 could for example extend from the outside of the magnetic shielding enclosure 41 to the inside of the magnetic shielding enclosure 41. The first and/or second thermal and mechanical linkages 481 – 482 could then be placed inside of the magnetic shielding enclosure 41. Alternatively, one or both of the first and second thermal anchor points 221 – 222 could extend from the inside of the magnetic shielding enclosure 41 to the outside of the magnetic shielding enclosure 41. The first and/or second thermal and mechanical linkages 481 – 482 could then be placed outside of the magnetic shielding enclosure 41.

In all embodiments presented in figures 4a – 4d, the thermal and mechanical linkages 481 – 482 may facilitate a releasable mechanical connection between the processor assembly and the first and second cold plates 321 – 322. This connection can be made with any suitable mechanical fasteners.

5 The one or more first and second electrical connectors 25 and 35 may be located outside of the magnetic shielding enclosure 41. The magnetic shielding enclosure may then shield the quantum processor die 29 even from the magnetic field generated at the 25 & 35 interface. Figure 4d illustrates this alternative with an embodiment where the processor assembly corresponds to the one illustrated in figure 2a. In other words, the electrical
10 signal connection 24 is connected to the carrier 21 and to the first electrical connector 25 via the first and second thermal anchor points 221 and 222.

The first electrical connector 25 is located outside of the magnetic shielding enclosure 41. The second end 242 of the electrical signal connection 24 may comprise a cable which extends through an opening in the magnetic shielding enclosure 41 from the inside of the
15 magnetic shielding enclosure 41 to the outside of the magnetic shielding enclosure 41. This cable may form both the electrical connection 49 to the first electrical connector 25 and the thermal connection 47 between the first electrical connector 25 and the second thermal anchor point 222. Furthermore, the parts of the fixed cable connection 36 which are closest to the 25 & 35 electrical interface may also be thermally connected to the
20 second cold plate 322. This connection has not been illustrated in figure 322.

The first electrical connector 25 may also be brought outside of the magnetic shielding enclosure 41 if the processor assembly corresponds to the one illustrated in figure 2a. The magnetic shielding enclosure 41 may for example form a part of the processor assembly, so that the entire magnetic shielding enclosure 41 is installed into the cryostat 31 when
25 the processor assembly is installed in the cryostat. The entire enclosure 41 is then also removed from the cryostat 31 when the processor assembly is removed from the cryostat 31.

The embodiment illustrated in figure 4d may be combined with any other embodiment presented in this disclosure.

30 Furthermore, any of the embodiments illustrated in figures 3 or 4a – 4d may be combined with the embodiment illustrated in figure 2f. That is, the processor assembly may comprise one or more additional thermal anchor points (such as the third anchor point 223) and additional circuit elements that are thermally connected to these anchor points. The cryostat may comprise corresponding one or more additional cold plates, and each

additional thermal anchor point may thermally (and, optionally, mechanically) connected to a corresponding additional cold plate. All thermal and mechanical connection options presented above in the discussion of figures 4a – 4d apply also to the connections between the one or more additional thermal anchor points and the one or more additional cold plates.

Figures 5a and 5b illustrates the quantum computing arrangement in more practical detail, although the presentation is still schematic. Any embodiment presented in this disclosure may be implemented with the arrangements shown in figures 5a and 5b. Each reference number is in figures 5a – 5b used with the same meaning as in the preceding figures.

In Figure 5a the carrier 21 is thermally and mechanically connected to the first thermal anchor point 221 (the mechanical connection is optional because the carrier 21 could alternatively be supported by a different structure). The processor assembly is surrounded by a magnetic shielding enclosure (411 + 412). A first thermal and mechanical linkage 481 extends from the first thermal anchor point 221 to the outside of the magnetic shielding enclosure 411 + 412 and is there thermally and mechanically connected to the first cold plate 321.

The second thermal anchor point 222 is in this case connected via a second thermal and mechanical linkage 482 to the second cold plate 322 inside the magnetic shielding enclosure 411 + 412. The second cold plate 322 extends into the magnetic shielding enclosure 411 + 412. The upper part 412 of the magnetic shielding enclosure is a fixed structure inside the cryostat. The lower part 411 of the magnetic shielding enclosure is a removable part which can either be a part of the processor assembly or a separate part which can be attached to the upper part 412 after the processor assembly has been installed in the cryostat.

The cryostat comprises a dilution unit 51 which creates a temperature difference between the first (321) and second (322) cold plates.

Either the first (481) or the second (482) thermal and mechanical linkage could optionally be only a thermal linkage which does not provide mechanical support for the processor assembly. The other linkage (481 or 482) may provide all of the needed mechanical support.

Parts 21, 24, 25, 221, 222, 28, 411, 481, 482 may all be removable parts in figure 5a, while all other parts may be fixed parts. The first thermal and mechanical linkage 481 may for example be a cold finger or a flexible thermal braid. The cold finger or thermal braid may extend through the upper part 412 of the magnetic shielding enclosure.

5 The first thermal and mechanical linkage 481 is set to the temperature of the first cold plate 321 when thermal contact is established between these parts. The second thermal and mechanical linkage 482 is set to the temperature of the second cold plate 322 when thermal contact is established between these parts. Depending on the geometry of the device, the first thermal and mechanical linkage 481 may have to be routed close to the second thermal anchor point 222 when it is brought out of the magnetic shielding enclosure 411 + 421. The first thermal and mechanical linkage 481 may be covered with a Teflon coating to minimize radiative heat transmission from the second thermal anchor point 222 to the linkage 481.

10 Figure 5b illustrates an alternative embodiment where parts 21, 24, 25, 221, 222, 28, 411, 412 and 481 may be removable parts, while all other parts may be fixed parts. Unlike in figure 5a, the upper part 412 of the magnetic shielding enclosure is in this case also a removable part, while the second thermal and mechanical linkage 482 is not.

15 The second thermal anchor point 222 extends out of the magnetic shielding enclosure 411 + 412 in figure 5b, so that the thermal and mechanical connection to the second cold plate 322 is made outside of the magnetic shielding enclosure 411 + 412. In general, in any embodiment presented in this disclosure, either one (or both) of the first or second thermal anchor points (or any additional thermal anchor points that the processor assembly might contain) can extend out of the magnetic shielding enclosure.

20 It can be seen in figure 5b that it corresponds to figure 4d in that the first electrical connector 25 is located outside of the magnetic shielding enclosure 411 + 412. This has the benefit that a magnetic field generated at the electrical 25 & 35 interface will not disturb the operation of the quantum processor die (not illustrated in figure 5b) on the carrier 21. This allows a broader range of connectors to be used as the first (25) and second (35) electrical connectors. These connectors may for example be magnetic electrical connectors.

Figures 5d and 5e illustrate in more detail the arrangements that may be employed to place the first electrical connector 25 outside of the magnetic shielding enclosure 411 + 412 in either of the embodiments shown in figures 5a and 5b.

30 In figure 5d, the upper part 412 of the enclosure comprises straight tubular openings 413. The second end 242 of the electrical signal connection 24 may comprise rigid electrical elements which extend through the tubular openings 413 to the first electrical connector 25 (multiple electrical connectors are illustrated in figure 5d). Figure 5e illustrates an embodiment where the tubular openings 413 have a meandering shape. The second end

242 of the electrical signal connection 24 may in this case be a flexible cable which passes through the meandering tubular opening 413. It would also be possible to use a flexible cable in the straight tubular opening in figure 5d, and to build rigid meandering elements which extend through the meandering tubular opening 413 in figure 5e.

5 The second thermal anchor point 222 may be thermally connected to the electrical signal connection 24 immediately inside the magnetic shielding enclosure 412. Alternatively, the second thermal anchor point 222 may be located outside of the magnetic shielding enclosure and thermally and mechanically connected to the first electrical connector 25 outside of the magnetic shielding enclosure. This option is illustrated in figure 5c. The
10 upper part 412 of the shielding enclosure is a part of the processor assembly, so it can be removed from the cryogenic vacuum chamber. The second thermal anchor point 222 may be attached to the upper part of the shielding enclosure 412 on the outside of the shielding enclosure 412, as figure 5c illustrate. In other words, the shielding enclosure is in this case located between the second thermal anchor point 222 and the carrier 21.

15 This disclosure also describes a method for manufacturing a processor assembly. The method may comprise connecting a quantum processor die electrically to a carrier. The method may also comprise connecting a first end of an electrical signal connection electrically to the carrier.

The quantum processor die may be attached to the carrier for example by soldering or
20 bump bonding or thermocompression bonding. Alternatively, it may be attached by welding (for example ultrasonic welding, laser welding or spot welding) or by wire bonding. Other methods are also possible.

As mentioned previously, the first end of the electrical signal connection may be connected directly to the carrier, or it may be electrically connected to the carrier via the first thermal
25 anchor point. Any of the connection methods mentioned above may be used to attach the first end of the electrical signal connection either to the first thermal anchor point or to the carrier.

The attaching of the quantum processor die to the carrier may be performed before electrically connecting the first end of the electrical signal connection to the carrier.
30 Alternatively, the attaching of the quantum processor die to the carrier may be performed after electrically connecting the first end of the electrical signal connection to the carrier.

CLAIMS

1. A processor assembly for a quantum computer, comprising:
 - a carrier and at least one quantum processor die mounted on the carrier,
 - a first thermal anchor point which is in thermal contact with the carrier,
 - 5 – a first electrical connector,
 - an electrical signal connection which comprises a first end which is electrically connected to the carrier and a second end which is electrically connected to the first electrical connector,
- characterized** in that the processor assembly also comprises:
 - 10 – a second thermal anchor point, and the second thermal anchor point is thermally separated from the first thermal anchor point, and the second thermal anchor point is in thermal contact with the first electrical connector.
2. A processor assembly according to claim 1, wherein the electrical signal connection is made of a superconducting material.
- 15 3. A processor assembly according to any of claims 1-2, wherein the electrical signal connection comprises a coaxial cable.
4. A processor assembly according to any of claims 1-2, wherein the electrical signal connection comprises a wiring board, and the wiring board has a main surface, and the electrical signal connection comprises a conductor which is in the wiring board and extends substantially parallel to the main surface of the wiring board.
- 20 5. A processor assembly according to any of claims 1-2, wherein the electrical signal connection comprises a wiring board, and the wiring board has a main surface, and the electrical signal connection comprises a conductor which is in the wiring board and extends substantially orthogonally to the main surface of the wiring board.
- 25 6. A processor assembly according to any preceding claim, wherein the processor assembly also comprises

- one or more additional thermal anchor points which are thermally separated from the first thermal anchor point, thermally separated from the second thermal anchor point and thermally separated from each other.
- 5 7. A quantum computing arrangement comprising a processor assembly according to any of the preceding claims.
8. A quantum computing arrangement according to claim 7, wherein the quantum computing arrangement also comprises:
- a cryogenic vacuum chamber, wherein the processor assembly is inside the cryogenic vacuum chamber,
- 10 – a fixed cable connection which is inside the cryogenic vacuum chamber, wherein the fixed cable connection comprises a second electrical connector, and the second electrical connector is electrically connected to the first connector of the processor assembly,
- a first cold plate and a second cold plate which are inside the cryogenic vacuum
- 15 chamber, wherein the temperature of the first cold plate is lower than the temperature of the second cold plate,
- and the first cold plate is in thermal contact with the first thermal anchor point in the processor assembly, and the second cold plate is in thermal contact with the second thermal anchor point in the processor assembly.
- 20 9. A quantum computing arrangement according to claim 8, wherein the arrangement also comprises a magnetic-shielding enclosure which is inside the cryogenic vacuum chamber and at least partly surrounds the processor assembly.
10. A quantum computing arrangement according to claim 9, wherein
- the first cold plate is located outside of the magnetic shielding enclosure and
- 25 the first thermal anchor point is located inside the magnetic shielding enclosure, and
- the first thermal anchor point is thermally and mechanically connected to a first thermal and mechanical linkage inside the magnetic shielding enclosure, and the first thermal and mechanical linkage extends from the inside of the

magnetic shielding enclosure to the outside of the magnetic shielding enclosure, and the first thermal and mechanical linkage is thermally and mechanically connected to the first cold plate outside of the magnetic shielding enclosure.

- 5 11. A quantum computing arrangement according to any of claims 9-10, wherein the second cold plate extends from the outside of the magnetic shielding enclosure to the inside of the magnetic shielding enclosure, and the second thermal anchor point is thermally connected to the second cold plate inside the magnetic shielding enclosure with a second thermal and mechanical linkage.
- 10 12. A quantum computing arrangement according to any of claims 9-11, wherein the one or more first and second electrical connectors are located outside of the magnetic shielding enclosure.
13. A method for manufacturing a processor assembly according to claim 1, wherein the method comprises:
- 15 – connecting the quantum processor die electrically to the carrier, and
- connecting the first end of the electrical signal connection electrically to the carrier.
14. A method according to claim 13, wherein the attaching of the quantum processor die to the carrier is performed before electrically connecting the first end of the electrical signal connection to the carrier.
- 20 15. A method according to claim 13, wherein the attaching of the quantum processor die to the carrier is performed after electrically connecting the first end of the electrical signal connection to the carrier.