Claims

1. A data transmission circuit, comprising:

a data processing unit of a mode register, comprising a read command processing unit of the mode register, wherein the read command processing unit of the mode register is configured to generate a first clock signal according to a received read command of the mode register, a second clock signal, and a preset read latency signal;

a data memory unit of the mode register configured to output data of the mode register in response to the first clock signal; and

a data memory unit of an array region configured to receive data of the array region in response to a first pointer signal, and to output data of the array region in response to a second pointer signal;

wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

2. The data transmission circuit according to claim 1, wherein the data memory unit of the array region comprises a plurality of first memory units, wherein an output terminal of each of the plurality of first memory units is connected to the first node, wherein an input terminal of each of the plurality of first memory units is connected to a first data signal line, and wherein the first data signal line is configured to transmit data of the array region.

3. The data transmission circuit according to claim 2, wherein a driving clock frequency of the first pointer signal and a driving clock frequency of the second pointer signal are the same.

4. The data transmission circuit according to any one of claims 1-3, further comprising:

a serial-parallel conversion circuit, wherein an input terminal of the serial-to-parallel conversion circuit is connected to the first node; and

a data driving module connected to an output terminal of the serial-parallel conversion circuit, and configured to output data of the mode register or data of the array region.

5. The data transmission circuit according to any one of claims 1-3, wherein the data processing unit of the mode register further comprises:

a first-in first-out pointer processing unit configured to generate a third pointer signal and a fourth pointer signal in response to the read command of the mode register; and

a first-in first-out data processing unit connected to the first-in first-out pointer processing unit, the data memory unit of the mode register and the mode register, wherein the first-in first-out data processing unit is configured to read data of the mode register from the mode register in response to the third pointer signal and to output the data of the mode register to the data memory unit of the mode register in response to the fourth pointer signal;

wherein a driving clock frequency of the third pointer signal and a driving clock frequency of the fourth pointer signal are the same.

6. The data transmission circuit according to claim 5, further comprising:

a command decoding circuit comprising a first output terminal connected to an input terminal of the read command processing unit of the mode register and an input terminal of the first-in first-out pointer processing unit, wherein the command decoding circuit is configured to receive a read command, decode and judge whether the read command is a read command of the mode register; and wherein the command decoding circuit is configured to output the read command of the mode register in response to the read command being the read command of the mode register, and to generate an data read command of the array region in response to the read command not being the read command of the mode register; and

a data processing unit of the array region comprising an input terminal connected to a second output terminal of the command decoding circuit, wherein the data processing unit of the array region is configured to read data of the array region from a memory unit array in response to the data read command of the array region, and to provide the data of the array region to the data memory unit of the array region.

7. The data transmission circuit according to claim 5, wherein the first-in first-out data processing unit comprises:

a plurality of second memory units, wherein an output terminal of each of the plurality of second memory units is connected to a second node;

wherein each of the plurality of second memory units comprises a memory sub-unit and a driver, wherein an input terminal of the driver is connected to an output terminal of the memory sub-unit, wherein the memory sub-unit is configured to receive data of the mode register under

a driving of the third pointer signal, wherein the driver is configured to output data of the mode register under a driving of the fourth pointer signal;

wherein an input terminal of each memory sub-unit is connected to the mode register.

8. A data transmission circuit, comprising:

a controllable delay module configured to generate a preset read latency signal in response to a read command of a mode register;

a data processing unit of the mode register connected to the controllable delay module, wherein the data processing unit of the mode register is configured to read data of the mode register from the mode register in response to a read command of the mode register, wherein the data processing unit of the mode register is further configured to send the data of the mode register to a data memory unit of the mode register in response to the preset read latency signal; and

a data memory unit of the array region, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node, and wherein the data memory unit of the array region is configured to receive data of the array region in response to a first pointer signal, and to output the data of the array region in response to a second pointer signal;

wherein the data memory unit of the mode register is configured to output the data of the mode register in response to a first clock signal.

9. The data transmission circuit according to claim 8, wherein a time difference between a start time when the data processing unit of the mode register outputs the data of the mode register and a time when the controllable delay module receives the read command of the mode register is a first preset threshold.

10. The data transmission circuit according to claim 9, wherein the controllable delay module comprises:

a reference delay unit configured to generate an initial preset read latency signal in response to the read command of the mode register; and

a controllable delay unit connected to an output terminal of the reference delay unit and an input terminal of the data processing unit of the mode register, wherein the controllable delay

unit is configured to generate a preset read latency signal after delaying a preset delay time from a moment of receiving the initial preset read latency signal;

wherein a sum of an operation delay of the controllable delay unit and an operation delay of the reference delay unit is equal to the first preset threshold.

11. The data transmission circuit according to claim 10, wherein the controllable delay unit comprises at least two delay units connected in series;

wherein at least one of the delay units is connected in parallel with a first controllable switch unit;

wherein the data transmission circuit is configured to change the number of delay units connected in series between the reference delay unit and the data processing unit of the mode register in the controllable delay unit by controlling turn-on or turn-off of the respective first controllable switch unit, to adjust an operation delay of the controllable delay unit.

12. The data transmission circuit according to any one of claims 8-11, wherein the data memory unit of the array region comprises a plurality of first memory units, wherein an output terminal of each of the plurality of first memory units is connected to the first node, an input terminal of each of the plurality of first memory units is connected to a first data signal line, and wherein the first data signal line is configured to transmit the data of the array region;

wherein a driving clock frequency of the first pointer signal and a driving clock frequency of the second pointer signal are the same.

13. The data transmission circuit according to any one of claims 8-11, wherein the data processing unit of the mode register comprises:

a read command processing unit of the mode register configured to generate a first clock signal according to a received read command of the mode register, a second clock signal, and a preset read latency signal;

a first-in first-out pointer processing unit configured to generate a third pointer signal and a fourth pointer signal in response to the read command of the mode register; and

a first-in first-out data processing unit connected to both the first-in first-out pointer processing unit and the data memory unit of the mode register, wherein the first-in first-out data processing unit is configured to read data of the mode register from the mode register in

response to the third pointer signal, and to output the data of the mode register to the data memory unit of the mode register in response to the fourth pointer signal;

wherein a driving clock frequency of the third pointer signal and a driving clock frequency of the fourth pointer signal are the same.

14. The data transmission circuit according to claim 13, further comprising:

a command decoding circuit, comprising a first output terminal connected to an input terminal of the read command processing unit of the mode register and an input terminal of the first-in first-out pointer processing unit, wherein the command decoding circuit is configured to receive a read command, decode and judge whether the read command is a read command of the mode register; and wherein the command decoding circuit is configured to output the read command of the mode register in response to the read command being the read command of the mode register, and to generates a data read command of the array region in response to the read command not being the read command of the mode register; and

a data processing unit of the array region, comprising an input terminal connected to a second output terminal of the command decoding circuit, wherein the data processing unit of the array region is configured to read data of the array region from a memory unit array in response to the data read command of the array region, and to provide the data of the array region to the data memory unit of the array region.

15. A data transmission circuit, comprising:

a delay module configured to generate a preset read latency signal after delaying a first preset time from a moment of receiving a read command of the mode register;

a data processing unit of the mode register, connected to the delay module and configured to read data of the mode register from the mode register in response to the read command of the mode register, and to output the data of the mode register to the data memory unit of the mode register in response to the preset read latency signal; and

a data memory unit of an array region, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node; wherein the data memory unit of the array region is configured to receive data of the array region in response to a first pointer signal, and to output the data of the array region in response to a second pointer signal;

wherein the data memory unit of the mode register is configured to output data of the mode register in response to a first clock signal.

16. The data transmission circuit according to claim 15, wherein the delay module comprises:

a first delay unit configured to generate a first preset read latency signal after delaying a second preset time from a moment of receiving the read command of the mode register;

a second delay unit connected to an output terminal of the first delay unit and configured to generate a second preset read latency signal after delaying a third preset time from a moment of receiving the first preset read latency signal, wherein the third preset time is equal to an operation delay of a column selection control module; and

a third delay unit connected to both an output terminal of the second delay unit and an input terminal of the data processing unit of the mode register; wherein the third delay unit is configured to generate a preset read latency signal after delaying a fourth preset time from a moment of receiving the second preset read latency signal;

wherein, a sum of the second preset time, the third preset time and the fourth preset time is equal to the first preset time.

17. The data transmission circuit according to claim 16, wherein the third delay unit comprises:

a first sub-delay unit connected to the output terminal of the second delay unit, wherein the first sub-delay unit is configured to generate a third preset read latency signal after delaying a fifth preset time from a moment of receiving the second preset read latency signal, wherein the fifth preset time is equal to an operation delay of a read-write amplifier; and

a second sub-delay unit connected to an output terminal of the first sub-delay unit and the input terminal of the data processing unit of the mode register; wherein the second sub-delay unit is configured to generate the preset read latency signal after delaying a sixth preset time from a moment of receiving the third preset read latency signal; and

wherein a sum of the fifth preset time and the sixth preset time is equal to the fourth preset time;

wherein the data memory unit of the array region comprises a plurality of first memory units, and an output terminal of each of the plurality of first memory unit is connected to a first

node, wherein an input terminal of each of plurality of first memory units is connected to a first data signal line, and wherein the first data signal line is configured to transmit the data of the array region;

wherein a driving clock frequency of the first pointer signal and a driving clock frequency of the second pointer signal are the same.

18. The data transmission circuit according to any one of claims 15-17, wherein the data processing unit of the mode register comprises:

a read command processing unit of the mode register, configured to generate the first clock signal according to a received read command of the mode register, a second clock signal, and the preset read latency signal;

a first-in first-out pointer processing unit, configured to generate a third pointer signal and a fourth pointer signal in response to the read command of the mode register; and

a first-in first-out data processing unit connected to both the first-in first-out pointer processing unit and the data memory unit of the mode register, wherein the first-in first-out data processing unit is configured to read data of the mode register from the mode register in response to the third pointer signal, and to output the data of the mode register to the data memory unit of the mode register in response to the fourth pointer signal;

wherein a driving clock frequency of the third pointer signal and a driving clock frequency of the fourth pointer signal are the same.

19. The data transmission circuit according to claim 18, further comprising:

a command decoding circuit, comprising a first output terminal connected to an input terminal of the read command processing unit of the mode register and an input terminal of the first-in first-out pointer processing unit, wherein the command decoding circuit is configured to receive a read command, decode the read command and judge whether the read command is a read command of the mode register; and wherein the command decoding circuit is configured to output the read command of the mode register in response to the read command being the read command of the mode register, and to generates an data read command of the array region in response to the read command not being the read command of the mode register; and

a data processing unit of the array region, comprising an input terminal connected to a second output terminal of the command decoding circuit, wherein the data processing unit of the array region is configured to read data of the array region from a memory unit array in

response to the data read command of the array region and to provide the data of the array region to the data memory unit of the array region.

20. A memory device, comprising:

a memory unit array configured to store data of an array region;

a mode register configured to store data of the mode register; and

a data transmission circuit according to any one of claims 1-19.