

ABSTRACT

PRODUCTION OF REVERSED FLASH MEMORY DEVICE

This invention relates to the new reversed flash memory device which has improved electrical performance, yield and reliability because of better control of the dielectric interfaces resulting from first making the poly 2 control gate within the silicon substrate. The reverse structure is novel, as are the described process methods for forming the reverse stacking order.

Shallow trench isolation (STI) is first formed in the p-silicon substrate and encompasses the poly 2 control gate region; then the interpoly dielectric is grown/deposited on that single crystal silicon substrate. The floating poly 1 is formed on top of this uniform interpoly dielectric that has well-controlled surface smoothness. The tunnel oxide layer is formed on the floating poly 1 layer, and the source/drain is implanted on a straddling additional poly layer. There are fewer edges and associated stress weaknesses in the dielectric breakdown of both the reversed interpoly dielectric and the floating tunnel oxide. The results are improved electrical quality and more acceptable electrical parameters, including reversed flash memory devices with gate length dimensions below 0.35 microns.

(FIGURE 4 IS SUGGESTED FOR PUBLICATION)