CLAIMS

1. A semiconductor device comprising:

a first active pattern, which is extended in a first direction, on a substrate;

a second active pattern, which is extended in the first direction and spaced apart from the first active pattern in a second direction, on the substrate;

a field insulating layer between the first active pattern and the second active pattern on the substrate;

a first gate electrode on the first active pattern;

a second gate electrode on the second active pattern;

a gate isolation structure separating the first gate electrode and the second gate electrode from each other on the field insulating layer; and

a gate insulating layer between the first gate electrode and the first active pattern,

wherein the gate isolation structure comprises a lower isolation pattern which is in contact with the field insulating layer, and an upper isolation pattern on the lower isolation pattern,

wherein the lower isolation pattern comprises a first portion, and a second portion below the first portion,

wherein in the first portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction increases in a downward direction from the upper isolation pattern,

wherein in the second portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction decreases in the downward direction from the upper isolation pattern, and

wherein the gate insulating layer extends along a sidewall of the lower isolation pattern to a level of an upper surface of the lower isolation pattern.

2. The semiconductor device of claim 1, wherein the lower isolation pattern further comprises a third portion between the first portion of the lower isolation pattern and the second portion of the lower isolation pattern, and

wherein in the third portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction is constant in the downward direction from the upper isolation pattern.

3. The semiconductor device of claim 2, wherein the lower isolation pattern further comprises a fourth portion between the third portion of the lower isolation pattern and the second portion of the lower isolation pattern, and

wherein in the fourth portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction increases in the downward direction from the upper isolation pattern.

4. The semiconductor device of claim 1, wherein the lower isolation pattern further comprises a third portion and a fourth portion, which are between the first portion of the lower isolation pattern and the second portion of the lower isolation pattern,

wherein the third portion of the lower isolation pattern is between the first portion of the lower isolation pattern and the fourth portion of the lower isolation pattern,

wherein in the third portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction decreases in the downward direction from the upper isolation pattern, and

wherein in the fourth portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction increases in the downward direction from the upper

isolation pattern.

5. The semiconductor device of any one of claims 1 to 4,

wherein the gate insulating layer extends along a portion of a sidewall of the upper isolation pattern.

6. The semiconductor device of any one of claims 1 to 4,

wherein the gate insulating layer is not on a sidewall of the upper isolation pattern.

7. The semiconductor device of any one of claims 1 to 6, wherein the upper isolation pattern comprises a first portion protruded above a level of an upper surface of the first gate electrode and a level of an upper surface of the second gate electrode, and

wherein in the first portion of the upper isolation pattern, a width of the upper isolation pattern in the second direction increases in an upward direction from the lower isolation pattern.

8. The semiconductor device of claim 7, wherein the upper isolation pattern further comprises a second portion below the first portion of the upper isolation pattern, and

wherein in the second portion of the upper isolation pattern, a width of the upper isolation pattern in the second direction increases and then decreases in the upward direction from the lower isolation pattern.

9. The semiconductor device of any one of claims 1 to 8, wherein each of the first active pattern and the second active pattern comprises a lower pattern protruded from the substrate, and a plurality of sheet patterns spaced apart from the lower pattern.

10. A semiconductor device comprising:

a first active pattern and a second active pattern, which are in a first region of a substrate and spaced apart from each other in a first direction by a first interval;

a third active pattern and a fourth active pattern, which are in a second region of the substrate and spaced apart from each other in a second direction by a second interval different from the first interval;

a first field insulating layer between the first active pattern and the second active pattern on the substrate;

a second field insulating layer between the third active pattern and the fourth active pattern on the substrate;

a first gate electrode on the first active pattern;

a second gate electrode on the second active pattern;

a third gate electrode on the third active pattern;

a fourth gate electrode on the fourth active pattern;

a first gate isolation structure separating the first gate electrode and the second gate electrode from each other on the first field insulating layer; and

a second gate isolation structure separating the third gate electrode and the fourth gate electrode on the second field insulating layer,

wherein the first gate isolation structure comprises a lower isolation pattern, which is in contact with the first field insulating layer, and an upper isolation pattern on the lower isolation pattern, and

wherein the second gate isolation structure is formed of a single structure extended from above an upper surface of the third gate electrode to below an upper surface of the second field insulating layer.

11. The semiconductor device of claim 10, wherein the second interval is greater than the first interval.

12. The semiconductor device of claim 10 or claim 11, wherein the upper isolation pattern of the first gate isolation structure comprises the same material as that of the second gate isolation structure.

13. The semiconductor device of any one of claims 10 to 12, wherein the lower isolation pattern of the first gate isolation structure comprises an upper region above a level of an upper surface of the first field insulating layer and a lower region below the level of the upper surface of the first field insulating layer, and

wherein in at least a portion of the upper region of the lower isolation pattern, a width of the lower isolation pattern in the first direction increases in a downward direction from the upper isolation pattern.

14. The semiconductor device of claim 13, wherein, in the upper region of the lower isolation pattern, a width of the lower isolation pattern in the first direction increases and then decreases in the downward direction from the upper isolation pattern.

15. The semiconductor device of claim 13, wherein, in the upper region of the lower isolation pattern, a width of the lower isolation pattern in the first direction increases and then remains constant in the downward direction from the upper isolation pattern.

16. A semiconductor device comprising:

a first active pattern, which comprises a first lower pattern extended in a first direction and a plurality of first sheet patterns spaced apart from the first lower pattern, on a substrate;

a second active pattern, which comprises a second lower pattern extended in the first direction and a plurality of second sheet patterns spaced apart from the second lower pattern, on the substrate, the second lower pattern being spaced apart from the first lower pattern in a second direction different from the first direction;

a field insulating layer between the first lower pattern and the second lower pattern on the substrate;

a first gate electrode on the first active pattern;

a second gate electrode on the second active pattern;

a gate isolation structure separating the first gate electrode and the second gate electrode from each other on the field insulating layer; and

a gate insulating layer between the first gate electrode and the first active pattern,

wherein the gate isolation structure comprises a lower isolation pattern that is in contact with the field insulating layer, and an upper isolation pattern on the lower isolation pattern,

wherein the lower isolation pattern comprises a material different from that of the upper isolation pattern,

wherein the lower isolation pattern comprises a first portion above a level of an upper surface of the field insulating layer,

wherein in the first portion of the lower isolation pattern, a width of the lower isolation pattern in the second direction increases in a downward direction from the upper isolation pattern,

wherein the upper isolation pattern comprises a first portion protruded above a level of an upper surface of the first gate electrode and a level of an upper surface of the second

gate electrode,

wherein in the first portion of the upper isolation pattern, a width of the upper isolation pattern in the second direction increases in an upward direction from the lower isolation pattern, and

wherein the gate insulating layer extends along a sidewall of the lower isolation pattern to a level of an upper surface of the lower isolation pattern.

17. The semiconductor device of claim 16, wherein the upper isolation pattern further comprises a second portion below the first portion of the upper isolation pattern, and

wherein in the second portion of the upper isolation pattern, a width of the upper isolation pattern in the second direction increases and then decreases in the upward direction from the lower isolation pattern.

18. The semiconductor device of claim 16 or claim 17,

wherein the gate insulating layer extends along a portion of a sidewall of the upper isolation pattern.

19. The semiconductor device of claim 16 or claim 17,

wherein the gate insulating layer is not on a sidewall of the upper isolation pattern.

20. The semiconductor device of any one of claims 16 to 19, wherein the lower isolation pattern comprises a lower region below the level of the upper surface of the field insulating layer, and

wherein in the lower region of the lower isolation pattern, a width of the lower isolation pattern in the second direction increases and then decreases as it moves away from

the upper isolation pattern.