WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor structure, comprising:

providing a substrate and a plurality of discrete bit line structures located on the substrate, the bit line structure having a metal layer therein, a top surface of the metal layer being lower than a top surface of the bit line structure;

forming a first isolation film filled between the adjacent bit line structures, a top surface of the first isolation film being higher than the top surface of the metal layer and lower than the top surface of the bit line structure, wherein the forming a first isolation film filled between the adjacent bit line structures comprises: forming an initial isolation film completely filled between the adjacent bit line structures; performing a flattening process to enable a top surface of the initial isolation film to be flush with the top surface of the bit line structure; and etching to remove a part of a thickness of the initial isolation film to form the first isolation film;

forming a first dielectric film on the top and sidewalls of the bit line structure and on the top surface of the first isolation film; and

etching to remove the first dielectric film on the top of the bit line structures and the top surface of the first isolation film by a maskless dry etching process to form a first dielectric layer, and etching to remove the first isolation film exposed by the first dielectric layer to form a first isolation layer exactly below the first dielectric layer.

2. The method according to claim 1, wherein a dielectric constant of a material of the first isolation layer is less than a dielectric constant of a material of the first dielectric layer.

3. The method according to claim 2, wherein the material of the first isolation layer comprises silicon dioxide, and a precursor gas forming the first

isolation layer comprises ethyl silicate and ozone.

4. The method according to claim 3, wherein the first isolation film is formed by a chemical vapor deposition process, and the first dielectric film is formed by an atomic layer deposition process.

5. The method according to claim 1, wherein a material of the first isolation layer comprises silicon; and after forming the first isolation layer, the first isolation layer is oxidized to generate silicon dioxide.

6. The method according to claim 5, wherein after forming the first isolation layer, the method further comprises: forming a second dielectric layer on a sidewall of the first isolation layer exposed by the first dielectric layer, a hardness of a material of the second dielectric layer being greater than a hardness of the material of the first isolation layer.

7. The method according to claim 1, wherein the process step of forming the first isolation layer and the first dielectric layer comprises: forming the first dielectric layer by a first maskless dry etching process, an etching rate of the first maskless dry etching process for the first dielectric film being greater than an etching rate for the first isolation film; and forming the first isolation layer by a second maskless dry etching process, the etching rate of the first maskless dry etching process for the first isolation film being greater than the etching rate for the first dielectric film.

8. The method according to claim 7, wherein the first isolation film comprises first regions located on sidewalls of the bit line structure and having a preset thickness, and a second region located between the first regions; and prior to performing the second maskless dry etching process, an ion doping process is performed on the first regions or the second region, the ion doping

process being configured to make the etching rate for the second region greater than the etching rate for the first regions.

9. The method according to claim 1, wherein a difference in height between the top surface of the first isolation film and the top surface of the bit line structure is 50 nm to 100 nm.

10. A semiconductor structure manufactured by the method as claimed in any of claims 1-9, comprising:

a substrate and a plurality of discrete bit line structures located on the substrate, the bit line structure having a metal layer therein, a top surface of the metal layer being lower than a top surface of the bit line structure;

a first isolation layer located on sidewalls of the bit line structure, a top surface of the first isolation layer being higher than the top surface of the metal layer and lower than the top surface of the bit line structure, wherein the material of the first isolation layer is silicon dioxide; and

a first dielectric layer located on sidewalls of the bit line structure and exactly above the first isolation layer.

11. The structure according to claim 10, wherein a dielectric constant of a material of the first isolation layer is less than a dielectric constant of a material of the first dielectric layer.

12. The structure according to claim 10, further comprising: a second dielectric layer located on sidewalls of the first isolation layer exposed by the first dielectric layer, a hardness of the material of the second dielectric layer being greater than a hardness of the material of the first isolation layer.