ABSTRACT

A METHOD TO FORM SHALLOW TRENCH ISOLATIONS WITH ROUNDED CORNERS AND REDUCED TRENCH OXIDE RECESS

A method of fabricating shallow trench isolations has been achieved. A semiconductor substrate is provided. A pad oxide layer is grown overlying the semiconductor substrate. A silicon nitride layer is deposited. The silicon nitride layer and the pad oxide layer are patterned to form a hard mask. The openings in the hard mask correspond to planned trenches in the semiconductor substrate. A silicon dioxide layer is deposited overlying the silicon nitride layer and the semiconductor substrate. The silicon dioxide layer is anisotropically etched to form sidewall spacers on the inside of the openings of the hard mask. The semiconductor substrate is etched to form the trenches. The sidewall spacers are etched away. The semiconductor substrate is sputter etched to round the corners of the trenches. An oxide trench lining layer is grown overlying the semiconductor substrate. A trench fill layer is deposited overlying the silicon nitride layer and filling the trenches. The trench fill layer is polished down to the top surface of the silicon nitride layer. The silicon nitride layer is etched away. The trench fill layer and the pad oxide layer are polished down to the top surface of the semiconductor substrate to complete the shallow trench isolation, and the integrated circuit device is completed.

(FIGURE 6 IS SUGGESTED FOR PUBLICATION)