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WHAT IS CLAIMED IS:

1. A memory controller comprising:

a programmable interface configured to receive a configuration signal into the memory controller indicating a selected address configuration; and

5 address circuitry coupled to the programmable interface and configured to process system addresses based on the selected address configuration to generate memory addresses.

2. A memory controller as claimed in claim 1, wherein the address circuitry is

10 configured to select bit groups from the system addresses based on the selected memory configuration to generate the memory addresses.

3. A memory controller as claimed in claim 1 or claim 2, wherein the configuration signal also indicates a selected memory configuration and the address circuitry is further
15 configured to process the system addresses based on the selected memory configuration to generate memory device selections.

4. A memory controller as claimed in claim 1, claim 2 or claim 3, wherein the address circuitry is further configured to receive the system addresses into the memory
20 controller and transfer the memory addresses from the memory controller and further comprising:

control circuitry configured to receive system control signals into the memory controller, generate memory control signals in response to the system control signals, and transfer the memory control signals from the memory controller; and

25 data circuitry configured to receive data into the memory controller and transfer the data from the memory controller.



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5. A memory controller as claimed in any of the preceding claims, wherein the address circuitry is configured to generate the memory addresses for a dynamic random access memory.

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6. A method of operating a memory controller, the method comprising:
receiving a configuration signal into the memory controller indicating a selected address configuration; and
processing system addresses based on the selected address configuration to
10 generate memory addresses.

7. A method as claimed in claim 6, wherein processing the system addresses to generate the memory addresses comprises selecting bit groups from the system addresses based on the selected memory configuration.

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8. A method as claimed in claim 6 or claim 7, wherein the configuration signal also indicates a selected memory configuration and further comprising processing the system addresses based on the selected memory configuration to generate memory device selections.

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9. A method as claimed in claim 6, claim 7 or claim 8, further comprising:
receiving system control signals and the system addresses into the memory controller;

generating memory control signals in response to the system control signals;
transferring the memory control signals and the memory addresses from the
memory controller; and
receiving data into the memory controller and transferring the data from the
5 memory controller.

10. A method as claimed in any one of claims 6 to 9, wherein processing the system
addresses to generate the memory addresses comprises generating the memory
addresses for a dynamic random access memory.

10 11. A memory controller as described herein with reference to Figures 1, 5 and 6.

12. A memory system as described herein with reference to Figure 1.

15 13. A method of operating a memory controller as described herein with reference to
Figures 2 and 3.

14. A method of manufacturing a memory system as described herein with reference
to Figure 4.