ABSTRACT

METHOD OF FORMING A POCKET IMPLANT REGION AFTER FORMATION OF COMPOSITE INSULATOR SPACERS

A process for forming a MOSFET device featuring a pocket region placed adjacent to only a top portion of the sides of a heavily doped source/drain region, has been developed. The process features forming a heavily doped source/drain region in an area of a semiconductor substrate not covered by the gate structure or by composite insulator spacers located on the sides of the gate structure. Selective removal of an overlying insulator component of the composite insulator spacer allows a subsequent pocket implant region to be formed in an area of the semiconductor substrate directly underlying a horizontal portion of a remaining L shaped insulator spacer component. The location of the pocket region, formed butting only the top portions of the sides of the heavily doped source/drain region, reduces the risk of punch through current while limiting the impact of junction capacitance.

FIGURE 6