

A time division multiple access digital transmission system, and a station for use in such a system.

The present invention relates to a time division multiple access digital transmission system comprising at least one primary station and a plurality of secondary stations, in which system the primary station transmits information to the secondary stations in frames comprising synchronisation information, and comprising user information in time slots, and in which system the secondary stations comprise a reference clock signal generator. Such a transmission system can be a mobile radio system, a cordless telephony system, or the like, or any system of the above kind in which primary and secondary stations have to be synchronised with respect to each other.

The present invention further relates to a secondary station for use in such a system.

A time division multiple access digital transmission system of this kind is known from the handbook "The GSM System for Mobile Communications", M. Mouly et al, published by the authors, 1992, pp. 195-216, pp. 227-241, and from the handbook "Mobile Radio Communications", R. Steele, Pentech Press, 1992, pp. 696-698. In this handbooks a TDMA (Time Division Multiple Access) mobile radio system, a so-called GSM system (Global System for Mobile Communications), and synchronisation of a mobile radio station MS to a radio base station BS in such a GSM system is described. Although in general terms synchronisation is described, as according to the GSM Recommendation GSM 05.10, in which it is prescribed for example that the mobile radio station carrier frequency shall be accurate to within 0.1 ppm (parts per million), or accurate to within 0.1 ppm compared to signals received from the radio base station, the GSM Recommendations do not specify the BS-MS synchronisation algorithms to be used, these being left to the equipment manufacturers. In hitherto GSM systems, synchronisation of a mobile radio station to a received datastream in time slots of TDMA frames may occur via two separate control loops. One control loop determines a time slot delay between a received time slot position intended for the mobile radio station and an expected time slot position. When an expected time slot position does not agree with the received time slot position, the expected time slot position is

corrected with the difference between the two. Another control loop evaluates the frequency offset between a received carrier frequency, and an expected received carrier frequency with respect to the frequency of a reference clock signal in the mobile radio station. The determined frequency offset is used to correct the frequency of the reference clock signal generator. A time slot sampling clock for an intermediate frequency or a base band signal derived from a received burst signal, and a data clock for clocking received data samples to a speech decoder, are derived from the reference clock signal. Due to the fact that both, independently operating, control loops control are acting upon the same cause, i.e. a Doppler effect causing varying symbol delays in the transmission channel between the radio base station and the mobile station, and instability of the reference clock signal generator, the data clock may shift with respect to the time slot sampling clock. This leads to a data sample slip causing a discrepancy between reading in/out of an input-output-buffer for speech samples acquired from/to be submitted to signal bursts or time slots, and the operation of a speech decoder/coder. Due to such a discrepancy, speech data may be lost. When other data than speech data, e.g. computer data or FAX data or exchanged between the radio base station and the mobile radio station, the data clock slip may even give rise to an unacceptable situation. Another solution can be that the data clock is not derived from the reference clock signal, but is controlled separately. Such a solution would give rise to more complex hardware.

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It is an object of the present invention to provide a time division multiple access digital transmission system of the above kind not having the drawbacks of known systems as to synchronisation.

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To this end the time division multiple access digital transmission system according to the present invention is characterised in that a secondary station comprises time slot delay determining means for determining a time slot delay between a received time slot position for the secondary station and an expected time slot position, and conversion means for converting the determined time slot delay into a first frequency offset, which is included into an adjustment signal for adjusting a frequency of the reference clock signal generator. It is achieved that all clocks in the secondary station can be derived from the reference clock signal generator, without giving rise to an unacceptable data slip, causing lost data.

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The present invention is based upon the insight that the first frequency offset as derived from the determined time slot delay is a measure for the frequency offset

between the primary station and the secondary station, independent of the cause of such an offset. Such a cause may be a frequency instability of the reference clock signal generator in the secondary station, a varying symbol delay in the transmission channel between the primary and the secondary station, a Doppler shift due to a secondary station moving away
5 from a primary station, or the like.

In an embodiment of a time division multiple access digital transmission system according to the present invention, the adjustment signal is a function of the determined first frequency offset and the determined time slot delay. With a proper choice of the function, e.g. a proportionality function, the determined time slot delay can virtually be
10 controlled to zero.

In an embodiment of a time division multiple access digital transmission system according to the present invention, a time slot sampling clock and a data clock, comprised in the secondary station, are derived from a reference clock signal. Herewith, data slip is effectively counteracted.

15 In an embodiment of a time division multiple access digital transmission system according to the present invention, determined time slot delays are filtered by means of a smoothing filter before being included into the adjustment signal. Herewith, the requirements of GSM Recommendation 05.10 can be fulfilled.

In an embodiment of a time division multiple access digital transmission
20 system according to the present invention, the system is modified in that the adjustment signal includes a second frequency offset signal instead of the first frequency offset signal, in case of an expected discontinuity in the determined time slot delay, the second frequency offset signal being a signal which is proportional to a received carrier signal frequency and an expected received carrier frequency. Herewith, also situations like initial synchronisation,
25 or a time slot change in case of handover, can be dealt with.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein

30 Fig. 1 schematically shows a time division multiple access digital transmission system according to the present invention,

Fig. 2 shows a secondary station according to the present invention, for use in such a system,

Fig. 3 shows a received frame structure in a secondary station according

to the present invention, with a time slot sampling clock and a data clock, and

Fig. 4A shows characteristics for determining an adjustment signal according to the present invention, for a constant time slot delay,

Fig. 4B shows characteristics for determining an adjustment signal according to the present invention, for a constant derivate of the time slot delay,

Fig. 4C shows 3-dimensional characteristics for determining an adjustment signal according to the present invention,

Fig. 5 shows a block diagram of speech paths in the secondary station, and

Fig. 6 shows a block diagram of a speech (de)coder in the speech paths.

Throughout the figures the same reference numerals are used for the same features.

Fig. 1 schematically shows a time division multiple access digital transmission system 1, for example a cellular mobile radio system like a GSM (Global System for Mobile Telecommunications) system as defined by ETSI (European Telecommunications Standards Institute), comprising in cells ce1, ce2 and ce3 radio base stations BS1, BS2 and BS3 as primary stations, for covering radio communication in the respective cells ce1, ce2 and ce3. In order not to cause interference with neighbouring cells the radio base stations, at least in adjacent cells, transmit and receive at different frequencies, usually each radio base station BS1, BS2 and BS3 transmitting and receiving at a number of frequencies, e.g. twelve frequency channels. By applying time division multiplex, such as TDMA, in GSM with eight time slots per frequency channel, 96 logical channels are available for radio communication per base station, then. The radio base stations BS1, BS2 and BS3 communicate with mobile radio stations MS1, MS2 and MS3 as secondary stations, the mobile radio stations being present in their respective cells, in the given example the radio base station BS1 communicating with the mobile stations MS1 and MS2, and the radio base station BS2 communicating with the mobile station MS3. When mobile radio stations are roaming through the cells ce1, ce2 and ce3 a so-called handover from one radio base station to another should occur if the quality of the communication link deteriorates, a system control function being carried out by a Mobile Switching Centre MSC, which is connected to the radio base stations BS1, BS2 and BS3 by means of landlines l1, l2 and l3 respectively. The MSC is connected to a Public Switched Telephone Network PSTN, in case of Public

Mobile Radio. For Private Mobile Radio, such connection can be deferred with.

Furthermore, in a GSM system, to protect the data from transmission errors on the radio path, among other operations, channel coding is applied on the logical channels before

transmission and channel decoding at reception, i.e. a lot of (quasi) real time processing is

5 required on data to be transmitted. To this end, and for other processing tasks, the radio base stations comprise a number of processors, and a number of channel codecs, channel encoders and decoders (not shown in detail here). For a more detailed description of a cellular system, e.g. GSM, referred is to said handbooks of Mouly and Steel.

Fig. 2 shows a secondary station MS1 according to the present invention,
10 for use in the TDMA digital transmission system 1, having a receiving branch Rx and a transmitting branch Tx. The secondary station MS1 comprises a voltage controlled oscillator 20 as a reference clock signal generator, an output 21 of which is coupled to a channel synthesizer 22. A channel number control signal chn can be fed to the channel synthesizer 22 for selecting a channel. Such a channel number control number chn is provided by a
15 processor (not shown) programmed for operating the secondary station MS1 in a known way, no further details being given as to known operating functions of the secondary station MS1. An output 23 of the synthesizer 22 is coupled to a first mixer 24 of the receiving branch 24, and to a second mixer 25 of the transmitting branch Tx. The reference clock signal generator 20 provides a data clock dcl via a first divider 26 which is coupled to a first phase offset
20 adder 27 for adding a data offset signal dof in case of an external synchronisation. Such an internal synchronisation is carried out in case of a discontinuous change of a received time slot position in the secondary station MS1, e.g. with initial synchronisation of the secondary station MS1 to the primary station BS1, or with a handover. With such an external synchronisation data clock synchronisation cannot be guaranteed, but at such an instant data
25 clock synchronisation is not necessary. The reference clock signal generator 20 further provides a time slot sampling clock tcl via a second divider 28, and a time slot control signal tct via a third divider 29 which is coupled to a second phase offset adder 30 for adding a mean determined time slot delay TOI_m as determined according to the present invention, in case of an external synchronisation. The time slot control signal tct is also fed to a third
30 phase offset adder 31 which is coupled to a modulator 32 in the transmitter branch Tx, a transmitting offset signal tof being applied to the offset adder 31. Switches 33, 34, and 35 are provided for switching over from a synchronisation of the secondary station MS1 as according to the present invention to an external synchronisation, known per se. The switches 33, 34, and 35 are shown in a synchronisation state as according to the present

invention. The time slot control signal tct controls a switch 36 which couples a filter 37 in the receiving branch Rx to an analog-to-digital converter 38, the filter 37 providing an intermediate frequency signal IF. Instead of an intermediate signal IF, a base band signal can be provided by the filter 37, this depending on the type of secondary station MS1, either

5 having a IF-receiver front end whereby base band conversion is carried out in a further stage (not shown), or having a direct-conversion front end (not shown). The intermediate frequency signal is sampled in an expected time slot position by the analog-to-digital converter 38, the expected time slot position being derived from information received at initial synchronisation, e.g. see pp. 214-216 of said handbook of Mouly. An output 39 of the

10 analog-to-digital converter 38 is coupled to an equalizer/demodulator arrangement 40, e.g. implemented as a programmed signal processor (not shown), the equalizer/demodulator 40 determining a time slot delay TOI which is a delay between a received time slot position and the expected time slot position, this information to be used as according to the present invention, and determining a frequency offset signal FOI, this information to be used in case

15 of an external synchronisation. In the latter case, the signal FOI is fed to a first integrator 41, an output 42 of which being coupled to the switch 35. The equalizer/demodulator 40, providing demodulated data dda, may determine the received time slot position from a received training sequence by means of a cross correlation of the received training sequence with a known transmitted bit pattern of the training sequence, the training sequence being

20 transmitted by the primary station BS1, together with transmitted data. The expected time slot position being known, because of the fact that the position of the training sequence within the time slot is known, the time slot delay TOI is determined as a deviation from the known position. According to the present invention, the determined time slot delay TOI is fed to a differentiating arrangement 43 after having been filtered with a low pass filter 44.

25 The determined time slot delay TOI is also fed to a second integrator 45 which smoothes the determined time slot delay TOI so as to form the mean determined time slot delay TOI_m . A differentiated determined time slot delay TOI_d and the mean or integrated determined time slot delay TOI_m are fed to a combiner arrangement 46 which provides an adjustment signal adj for adjusting the reference clock signal generator 20 to varying time slot delays such that

30 no unacceptable data clock slip occurs. The adjustment signal adj preferably is a function of the determined quantities TOI_d and TOI_m , e.g. a proportionality function. If $TOI_m = 0$, then $df = dTOI/dt = -adj$, d/dt being a differential operator. If $TOI_m < > 0$, then $adj = -df + k \cdot TOI_m$, $< >$ representing inequality, and k being a proportionality factor. By means of a computational block 47, a current value of a control value cti is determined, which is fed to

a digital-to-analog converter 48 that controls the reference clock signal generator 20, the current value being an addition of a previous value of the control value ctl and a previous value of the adjustment signal adj . According to the present invention, for control of the reference clock generator 20 in a situation of continuous control, i.e. no discontinuities in the mean delay TOI_m , no control via the offset FOI is necessary, because a frequency offset between a master oscillator (not shown) in the primary station BS1 and the reference clock signal generator in the secondary station is directly reflected into the delay TOI . A varying delay TOI , with time, corresponds to a frequency offset between the primary station BS1 and the secondary station MS1, and a mean delay $TOI_m < > 0$ indicates non-synchrony in the received time slot position. For short term averaging, the integrator 45 should have a time constant $\ll dt$.

Fig. 3 shows a received frame structure FR in the secondary station MS1 according to the present invention, showing positions of the time slot sampling clock tcl and the data clock dcl , with respect to each other. Shown is an uplink GSM multiframe of 26 frames, repetitively numbered F0 to F25, the multiframe FR having a duration of 120 msec. Such a multiframe structure is described on pp. 215-216 of said handbook of Mouly. In GSM, each TDMA frame of a multiframe structure has 8 time slots. Also, in GSM, information is transmitted in bursts having a finite duration, the bursts being transmitted in the time slots. Frame number F12 is a so-called SACCH (Slow Associated Control Channel) in GSM, providing control information for a number of consecutive time slots. Frame number F25 is an idle frame. At least 4 bursts are necessary to transmit 20 msec of coded speech information. Due to frame interleaving, as applied on the radio interface in GSM, 20 msec of coded speech information is distributed over 8 bursts. With horizontally hatched blocks, a computational time CMP for channel coders and speech coders (not shown) is indicated, such speech coders operating on segments of speech having a duration of 20 msec. Between two horizontally hatched blocks, a buffer (not shown) is filled by 160 samples for subsequent processing by a speech coder. As can be seen in Fig. 3, there is still a time margin MAR after computation, i.e. at the instant T1, before transmission instant TXR immediately following the instant T1, but it can also be seen that the two clock systems, i.e. the time slot sampling clock and the data clock, only allow for a small asynchronism or slip between the two clock systems. With secondary station MS1, as described in Fig. 2, no unacceptable slip, giving rise to data loss, normally occurs, all clocks being derived from the same reference clock signal generator 20.

Fig. 4A shows characteristics for determining an adjustment signal

according to the present invention, for a constant time slot delay. Shown are axes adj , df , and TOI_m , wherein $adj = f(TOI_m, df)$, for a constant mean time slot delay TOI_m . Shown are characteristics for $TOI_m = 0$, and for $TOI_m = C1$, $C1$ being a given constant value. In the shown 3-dimensional plane, positive adjustment signals adj are indicated with a solid line, and negative adjustment value adj are indicated with a dashed line. As an initial state, it is assumed that a transmitted burst by the primary station BS1 is expected at the switch 36 in the secondary station MS1 such that the time slot delay TOI and the derivate TOI_d of the time slot delay TOI are positive. With such an initial state, for a positive value of the signal FOI and for df is positive, the frequency of the reference clock signal generator 20 should be decreased, i.e. $adj < 0$, and for a positive value of the time slot delay TOI , the frequency of the reference clock signal generator 20 should be increased, i.e. $adj > 0$.

Fig. 4B shows characteristics for determining an adjustment signal according to the present invention, for a constant derivate TOI_d of the time slot delay TOI . Shown is a characteristic for $df = 0$, i.e. shown is a characteristic in the adj - TOI_m plane.

Fig. 4C shows 3-dimensional characteristics for determining the adjustment signal adj according to the present invention, in which $adj = f(TOI_m + df)$, the characteristics field taking system constraints into account, e.g. according to GSM Recommendations.

Fig. 5 shows a block diagram of speech paths in the secondary station MS1 according to the present invention. A speech path from the secondary station MS1 into the direction of the primary station BS1 comprises a microphone 50, an analog-to-digital converter 51, a speech coder 52, and a channel coder 53, coupled to the modulator 32. A speech path from the primary station BS1 into the direction of the secondary station MS1 comprises a channel decoder 54 coupled to the equalizer/demodulator 40, a speech decoder 55, a digital-to-analog converter 56, and a receiver 57. In Fig. 5, it is indicated at which parts of the secondary station MS1 the data clock dcl and the time slot sampling clock tcl operate.

Fig. 6 shows a block diagram of the speech coder 52, and the speech decoder 55, in the speech paths. The speech coder 52 comprises a buffer 60, which can comprise 160 speech samples (corresponding to 20 msec of speech) generated by the analog-to-digital converter 51, and further an intermediate buffer 61 for buffering 160 samples per 20 msec, and a speech coding algorithm comprised in a digital signal processor 62. Such an algorithm can be a known algorithm such as applied in a GSM system. Each time when the buffer 60 is full, its content is copied into the intermediate buffer 61. The speech decoder 55

comprises a speech synthesis algorithm in a digital signal processor 63, the algorithm being known per se, and further an intermediate buffer 64 for 160 samples per call of the speech decoder 63, and a buffer 65. Each time when the buffer 65 is empty, a copy of the contents of the intermediate buffer 64 is copied into the buffer 65. In Fig. 6, it is indicated at which
5 parts of the speech (de)coder the data clock dcl and the time slot sampling clock tcl operate.

CLAIMS:

1. A time division multiple access digital transmission system (1) comprising at least one primary station (BS1, BS2, BS3) and a plurality of secondary stations (MS1, MS2, MS3), in which system (1) the primary station (BS1, BS2, BS3) transmits information to the secondary stations (MS1, MS2, MS3) in frames (FR) comprising synchronisation information, and comprising user information in time slots, and in which system (1) the secondary stations (MS1, MS2, MS3) comprise a reference clock signal generator (20), characterised in that a secondary station (MS1, MS2, MS3) comprises time slot delay determining means (40) for determining a time slot delay (TOI) between a received time slot position for the secondary station and an expected time slot position, and conversion means (43) for converting the determined time slot delay (TOI) into a first frequency offset (TOI_d), which is included into an adjustment signal (adj) for adjusting a frequency of the reference clock signal generator (20).
2. A time division multiple access digital transmission system (1) according to claim 1, wherein the adjustment signal (1) is a function of the determined first frequency offset (TOI_d) and the determined time slot delay (TOI_m).
3. A time division multiple access digital transmission system (1) according to claim 2, wherein the function is a proportionality function.
4. A time division multiple access digital transmission system (1) according to claims 1, 2 or 3, wherein a time slot sampling clock (tcl) and a data clock (dcl), comprised in the secondary station (MS1, MS2, MS3), are derived from a reference clock signal (20).
5. A time division multiple access digital transmission system (1) according to claims 1, 2, 3 or 4, wherein determined time slot delays (TOI) are filtered by means of a smoothing filter (41) before being included into the adjustment signal (adj).
6. A time division multiple access digital transmission system (1) according to claim 1, modified in that the adjustment signal (adj) includes a second frequency offset signal (FOI) instead of the first frequency offset signal (TOI_d), in case of an expected discontinuity in the determined time slot delay, the second frequency offset signal (FOI) being a signal which is proportional to a received carrier signal frequency and an expected



received carrier frequency.

7. A time division multiple access digital transmission system (1) according to any one of the claims 1 to 6, the system being a mobile radio system.

8. A secondary station (ms1, ms2, ms3) for use in a time division multiple
5 access digital transmission system (1) in which a primary station (BS1, BS2, BS3) transmits information to secondary stations (MS1, MS2, MS3) in frames (FR) comprising synchronisation information, and comprising user information in time slots, and in which
system (1) the secondary stations (MS1, MS2, MS3) comprise a reference clock signal
generator (20), characterized in that the secondary station (MS1, MS2, MS3) comprises time
10 slot delay determining means (40) for determining a time slot delay (TOI) between a received time slot position for the secondary station and an expected time slot position, and conversion means (43) for converting the determined time slot delay into a first frequency offset (TOI_d), which is included into an adjustment signal (adj) for adjusting a frequency of the reference clock signal generator (20).

