

PARALLEL INSTRUCTION EXTRACTION METHOD AND READABLE STORAGE MEDIUM

ABSTRACT

The invention relates to the technical field of a processor, in particular
5 to a method for parallel extracting instructions and a readable storage
medium. The method generates a valid vector of fetched instructions
according to the end position vector s_mark_end of the instruction, and
performs parallel decoding of instructions at each position, calculation of
instruction address and branch instruction target address operation through
10 logical "AND" and logical "OR" operations. Ultimately, multiple instructions
are fetched in parallel. The present invention is a method for generating a
valid vector of fetching instructions according to the end position vector
s_mark_end of the instruction, and extracting multiple instructions in
parallel through logical "AND" and logical "OR" operations. The invention
15 can extract a plurality of instructions in parallel at the same time, there is no
serial dependence relationship between each instruction, and the time
sequence is easy to converge, so a higher main frequency can be obtained.
The invention is particularly suitable for high-performance processors that
extract more than 8 instructions per clock cycle.