

PATENT SPECIFICATION

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DRAWINGS ATTACHED



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(54) INTEGRATED CIRCUITS FOR AC LINE OPERATION

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a circuit which includes an integrated circuit chip, and more particularly, to such a circuit in which the chip can be directly coupled to a source of alternating current (a.c.) energy.

It is desirable in any circuit to minimize the number of separate components. The advantages include savings in cost, reduced weight and size, and increased reliability.

One obvious way in which these advantages may be realized is through the use of a junction isolated integrated circuit. However, most known such integrated circuits could only be used in an application in which an external direct current (d.c.) supply was used. It has not been safe to apply an a.c. supply power directly to a junction isolated integrated circuit chip because the isolation junction, which must be reverse biased for proper operation, can become forward biased. The circuit would thus be inoperative and possibly subject to catastrophic failure.

Thus, where one desired to use an integrated circuit to perform any desired function, it was preferred to avoid necessity to provide external d.c. power to the chip by means such as an external battery or external discrete elements connected as an a.c. to d.c. converter. This meant more external components, with the accompanying greater cost, weight, size, and decreased reliability.

In accordance with this invention there is provided a circuit comprising two input terminals, two output terminals, a semiconductor substrate of one conductivity type; a first semiconductor region of a material having a conductivity type opposite to that of said

substrate material, a portion of said first region being positioned adjacent said substrate such that a first rectifying junction is formed therebetween; a second semiconductor region of a material of said one conductivity type positioned within said portion of said first region; said first region portion and second region being direct current conductively coupled to one of said input terminals; a third semiconductive region of a material of said opposite conductivity type positioned within said second region such that a second rectifying junction is formed therebetween; a direct current connection between said third region and one of said output terminals; the other one of said input terminals being directly connected to the other one of said output terminals; another portion of said first region positioned with respect to said substrate such that a third rectifying junction is formed therebetween; a direct connection between said other input terminal and said other portion of said first region; said third rectifying junction acting to maintain the potential of said substrate substantially at the potential of said directly connected input and output terminals when said source is of a given polarity and to prevent said first rectifying junction from being forward biased when said source is of opposite polarity; said first region first-mentioned portion having an annular configuration with one end closed box-like by that section of said first region directly adjacent said substrate, said second and third regions being wholly within said annular configuration, and the concentrations of conductivity-determining impurities and the widths of said second region, first region portion, substrate, and other portion of said first region being selected so that the effective gain of the parasitic four layer diode formed by the mutually adjacent parts thereof is sufficiently low to render said parasitic diode substantially inoperative.

The invention will be more fully understood when reference is made to the accompanying drawings, in which:—

[Price 25p]

Figure 1 is a cross-section of a portion of a junction isolated integrated circuit according to one embodiment of the present invention; and

5 Figure 2 is a circuit diagram in conventional form of the circuit shown in Figure 1.

Referring to Figure 1, a portion is shown of a circuit 10 which includes a junction isolated integrated circuit chip 12 which may additionally include complex a.c. and d.c. processing circuitry (not shown). A.C. power, designated by the letters A.C. is to be applied from a suitable source (not shown) to terminals 14 and 16. If one considers terminal 15 14 as the reference terminal, the voltage at terminal 16 swings between a peak positive value and an equal peak negative value with respect to the reference. Terminal 14 is connected to one end of capacitor 18 and load 20 designated herein as a resistance R_L but which may be any type of circuit requiring the application of a source of d.c. power and which may be included on chip 12. Input terminal 16 is connected to one end of an external resistance 22. Integrated circuit chip 12 is connected between the other end of resistor 22 and the other ends of capacitor 18 and load 20.

Integrated circuit chip 12 includes a P type substrate 24 which has a diffused N+ region 26 therein. An epitaxial layer which includes a plurality of N type regions 28, 30, 31 and 32 is epitaxially grown on substrate 24; during the epitaxial growth process region 26 also diffuses into region 28. The regions 28, 30, 31, 32 are isolated from one another by diffused P+ regions 34, 36, and 38 in conjunction with the substrate 24.

Region 28 has diffused therein a P region 40 and an N+ ring 42 which surrounds the P region 40 and a portion of N layer 28. Ring 42 is made in two steps such that the deep diffused portion thereof 44 is made first and goes as far down as N+ region 26, then a shallow diffused portion 46 is formed. P region 40 has an N+ region 48 diffused therein.

N region 30 has an N+ region 50 diffused therein. These epitaxial and diffused regions are formed on the substrate in a known manner which need not be described herein.

Metallization in the form of conductive strips (which may be formed by evaporation or plating of a suitable metal such as aluminum) 52, 54, and 56 is also provided. Conductive strip 52 is connected respectively to P region 40 and N+ ring region 42 such that the two regions are shortcircuited. Conductive strip 54 is connected to N+ region 48, and conductive strip 56 is connected to N+ region 50. Strips 52, 54, 56, are separated from each other and the remainder of chip 12 by an insulating layer (which may for example comprise silicon dioxide or

silicon nitride) having portions 58, 60, 62, 64 and 66.

There is a connection between conductive strip 56 and the input terminal 14. The other end of resistor 22 is connected to conductive strip 52 and a connection is provided between the conductive strip 54 and the capacitor 18 and load 20.

Figure 2 shows a circuit diagram in conventional form of the structure shown in Figure 1 and, where possible, similar numbers have been used to designate similar components. In the integrated circuit chip 12, as shown by the dashed lines in Figure 2, there are two diodes 70 and 72. Diode 70 is formed on integrated circuit chip 12 by the junction of P region 40 and N+ region 48. Diode 72 is formed on chip 12 by the junction of N region 30 and the P substrate 24, with the diode 72 so formed being connected to terminal 14 via strip 56 and N+ contact region 50. In addition, a diode 74, formed between substrate 24 and regions 26 and 28 is shown in dotted lines because it is not a part of the circuit design, but is inherent in the use of a back-biased junction isolated integrated circuit.

The operation of circuit 10 will now be explained. When terminal 16 is more positive than terminal 14, diode 70 conducts and capacitor 18 is charged up to a positive voltage. During this time, the substrate 24 is prevented from rising above the reference potential at terminal 14 by diode 72. However, when terminal 14 becomes more positive with respect to terminal 16, the most negative point of the circuit is no longer at reference potential but rather at the potential of terminal 16 that is, the potential at terminal 16 drops below reference potential.

If diode 72 were not present and substrate 24 was connected directly to the reference potential at terminal 14, diode 74, formed by substrate 24 and region 26 would conduct because the cathode (region 26) of diode 74 is negative with respect to the anode (substrate 24). This would result in the circuit being inoperative and might result in catastrophic failure. However, since diode 72 is present, the current flow through diode 74 is blocked, that is, the substrate is effectively isolated from the reference or "floating". Thus, for the positive half cycle, substrate 24 is prevented from rising above reference potential and for the negative half cycle, it is "floating".

A further problem in any chip, in which a diode similar to diode 72 is present, is parasitic multi-layer device action. This problem exists because substrate 24 is common to all epitaxial regions, such as regions 28, 30, 31 and 32. Where any active device is present in an epitaxial region, there may exist a parasitic multi-layer device. One such device as shown by the dashed line in Figure

1 could consist of P region 40, N region 28, P substrate 24 and N region 30 if metal strip 52 did not short circuit N+ ring 42 and P region 40 as would be the case in a transistor. For example, a four layer device would also exist between N layer 30, P substrate 24 and the collector and base of any transistor structure in the remainder of the chip (not shown in Figure 1).

The presence of the box including N+ ring 42 and N+ region 26 prevents this parasitic four layer device from acting as a controlled rectifier by decreasing the internal loop gain of the device to less than one. Thus N+ ring 42 and N+ region 26 must be of sufficient thickness to reduce this loop gain below one. Structure similar to the box which includes N+ ring 42 and N+ region 26 is described in U.S. Patent 3,430,110.

Although the parasitic controlled rectifier action just described may not in practice be present in the circuit of Figure 1, the aforementioned box should be included to insure that it is not. Further, since other boxes similar to the box including N+ region 26 and N+ ring 42 will be diffused into the chip because of possible parasitic multilayer device action due to the presence of the diode formed by N region 30 and substrate 24 and the other active devices (not shown) on the chip, it is preferable to include N+ ring 42 and N+ region 26 as shown.

WHAT WE CLAIM IS:—

1. A circuit comprising two input terminals, two output terminals, a semiconductor substrate of one conductivity type; a first semiconductor region of a material having a conductivity type opposite to that of said substrate material, a portion of said first region being positioned adjacent said substrate such that a first rectifying junction is formed therebetween; a second semiconductor region of a material of said one conductivity type positioned within said portion of said first region; said first region portion and second region being direct current conductively coupled to one of said input terminals; a third semiconductive region of a material of said opposite conductivity type positioned within said second region such that a second rectifying junction is formed therebetween; a direct current connection between said third region and one of said output terminals; the other one of said input terminals being directly connected to the other one of said output terminals; another portion of said first region positioned with respect to said substrate such that a third rectifying junction is formed therebetween; a direct connection between said other input terminal

and said other portion of said first region; said third rectifying junction acting to maintain the potential of said substrate substantially at the potential of said directly connected input and output terminals when said source is of a given polarity and to prevent said first rectifying junction from being forward biased when said source is of opposite polarity; said first region first-mentioned portion having an annular configuration with one end closed box-like by that section of said first region directly adjacent said substrate, said second and third regions being wholly within said annular configuration, and the concentrations of conductivity-determining impurities and the widths of said second region, first region portion, substrate, and other portion of said first region being selected so that the effective gain of the parasitic four layer diode formed by the mutually adjacent parts thereof is sufficiently low to render said parasitic diode substantially inoperative.

2. A circuit according to claim 1 wherein the first semiconductor region has an epitaxial layer having a plurality of isolated zones of semiconductor material contained therein; one of said isolated zones comprising said first portion of said first region and said second and third regions; another of said isolated regions comprising said other portion of said first region; there being a connection between the other one of said input terminals and the other one of said output terminals over a path separate from said first, second and third rectifying junctions.

3. The circuit according to claim 2, wherein said first region first portion is highly doped with conductivity determining impurities.

4. The circuit according to claim 3, wherein said third region is highly doped with conductivity determining impurities.

5. The circuit according to any of claims 1—4 wherein said first portion of said first zone and said second region are electrically interconnected by a conductive strip.

6. The circuit according to claim 5 wherein said conductive strip is direct current connected through a resistor to said one input terminal.

7. A circuit substantially as hereinbefore described in conjunction with the accompanying drawing.

T. I. M. SMITH,
Chartered Patent Agent,
50 Curzon Street,
London, W1Y 8EU.
Agent for the Applicant.

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