What is claimed is:

1. A method of annealing a semiconductor product wafer having a back side with an annealing region, the product wafer having electronic device features that reside a distance d from the back side and that are subject to being damaged beyond a critical temperature T_C, the method ~~consisting~~ comprising of:

scanning a single annealing laser beam over the back side to anneal the annealing region by bringing the annealing region up to an anneal temperature T_A that is less than a melt temperature T_M of the semiconductor product wafer, wherein the annealing region is either ~~an~~ a semiconductor ion-implant layer or a semiconductor contact layer; and

wherein the scanning of the single annealing laser beam defines ~~the annealing region and has~~ a thermal diffusion length L_D attendant therewith, and further including performing said scanning with a dwell time such that a thermal diffusion length L_D satisfies $L_D < d$ and wherein the electronic device features are maintained below the critical temperature T_C.

2. The method according to claim 1, wherein the dwell time is in the range from 3 microseconds to 200 microseconds.

3. The method according to claim 1, wherein the electronic device features include metal and wherein the critical temperature T_C is in the range from 600°C to 900°C.

4. The method according to claim 1, wherein the semiconductor product wafer is constituted by a device wafer interfaced with a carrier wafer, wherein the device wafer includes the electronic device features that defines the distance d.

5. The method according to claim 4, wherein the single annealing laser beam has a visible wavelength or an infrared wavelength with an optical absorption length less than the thickness of the device wafer.

6. The method according to claim 1, wherein the electronic device features include a CMOS device layer.

7. The method according to claim 1, wherein the electronic device features include a semiconductor power-device layer.

8. The method according to claim 1, wherein said scanning includes performing multiple scans of the single annealing laser beam over a same portion of the back side, wherein temporally adjacent scans are separated in time by a time interval τ, and wherein 1 millisecond $\leq \tau \leq$ 10 seconds.

9. The method according to claim 8, wherein the number of multiple scans is 10 or fewer.

10. The method according to claim 1, wherein 5 μm $\leq d \leq$ 150 μm.

11. The method according to claim 1, wherein 10 μm $\leq d \leq$ 20 μm, the electrical device features are made of aluminum, and wherein the dwell time t_d is between 3 microseconds to 20 microseconds.

12. The method according to claim 1, wherein 10 μm $\leq d \leq$ 20 μm, the electrical device features are made of copper, and wherein the dwell time t_d is between 15 microseconds to 100 microseconds.

13. A method of annealing a product wafer, comprising:

forming a product wafer by forming a protective structure over a front side of a device wafer having a back side and a thickness d between 5 microns and 150 microns, wherein the front side includes electronic device features that are subject to being damaged if heated beyond a critical temperature T_C;

forming an annealing region in or on the back side of the device wafer, wherein the annealing region includes ~~an~~ a semiconductor ion-implanted doped

layer formed within the back side or a semiconductor contact layer formed on the back side; and

scanning a single annealing laser beam over the back side to perform non-melt annealing of the annealing region, wherein the scanning is performed with a dwell time that defines a thermal diffusion length $L_D < d$ and wherein the electronic device features are maintained at a temperature below the critical temperature T_C.

14. The method according to claim 13, further comprising performing multiple scans of a same portion of the back side with the single annealing laser beam, wherein temporally adjacent scans are separated by a time interval τ, and wherein 1 millisecond $\leq \tau \leq$ 10 seconds.

15. The method according to claim 14, wherein the number of multiple scans is 10 or fewer.

16. The method according to claim 13, wherein the protective structure includes a carrier wafer.

17. The method according to claim 13, wherein the protective structure consists of a single protective layer.

18. The method according to claim 13, wherein the electronic device features include at least one of a metal and a CMOS layer.

19. The method according to claim 13, wherein the electronic device features include a semiconductor power-device layer.

20. The method according to claim 13, wherein the dwell time is in the range from 3 microseconds to 200 microseconds.

21. The method according to claim 13, including selecting the dwell time to be less than a maximum dwell time t_{dm} defined by $t_{dm} = d^2/D_{eff}$, where D_{eff} is the effective thermal diffusivity of the device wafer.

22. The method according to claim 13, wherein the annealing laser beam has a visible wavelength or an infrared wavelength with an optical absorption length less than the thin-wafer thickness.

23. The method according to claim 13, wherein 10 μm ≤ d ≤ 20 μm, the electrical device features are made of aluminum, and wherein the dwell time t_d is between 3 microseconds to 20 microseconds.

24. The method according to claim 13, wherein 10 μm ≤ d ≤ 20 μm, the electrical device features are made of copper, and wherein the dwell time t_d is between 15 microseconds to 100 microseconds.